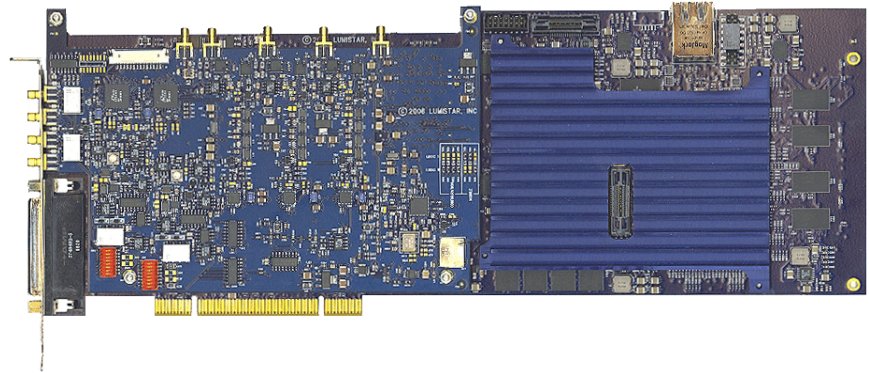


# LUMISTAR

## LS-34-BB Synchronization BEAST PCI Board Dual 35 Mbps Bit Synchronizers and Dual Multifunction Decoms Data Sheet

### Description:

The Lumistar LS-34-BB Synchronization Beast PCI Board is one application of the Lumistar BEAST family of programmable telemetry boards. The LS-34-BB consists of an Analog Front End daughterboard and a Digital Processing mainboard with up to 10 Million Gates of FPGA. The Analog Front End daughterboard provides the bit synchronizer pre-conditioning, two channels of high speed digitization, and the output data conditioning required for a high performance bit synchronizer. The Digital Processing mainboard contains two bit synchronizers with data rates up to 35 Mbps, and two multi-function decoms including time code readers, time code generators, PCM Simulators, pseudo-random bit stream generators (PRBS), and PCM Decoms.



The LS-34-BB provides optimal reconstruction of a serial PCM data stream that has been corrupted by noise, phase jitter, amplitude modulation, or base line variations. The all-digital design assures a consistent product with high reliability and long-term stability.

The Bit Synchronizer Analog Front End contains the pre-conditioning for impedance conversion, correction for baseline shift and variation, AGC control, and anti-alias filtering prior to the two channels of high speed A/D conversion.

### Key Features:

- Available in Single (LS-34-B) or Dual (LS-34-BB) channel configurations
- Specific configuration depends on firmware license purchased
  - Bit Synchronizers with data rates to 35 Mbps (NRZ)
  - Bit Synchronizers with Multi-function Decoms to 35 Mbps
  - Soft Bit Decision Outputs or internal Viterbi Decoding
- Analog Front End daughterboard performs Input and Output interface
- Digital Processing mainboard performs all functions in FPGA
- Mainboard processor uses Embedded Linux (independent of PCI bus)
- All-digital design assures high reliability and long term performance
- Dual Oscilloscope option allows eye pattern displays through software
- Dual DAC interface bus to LS-71 products

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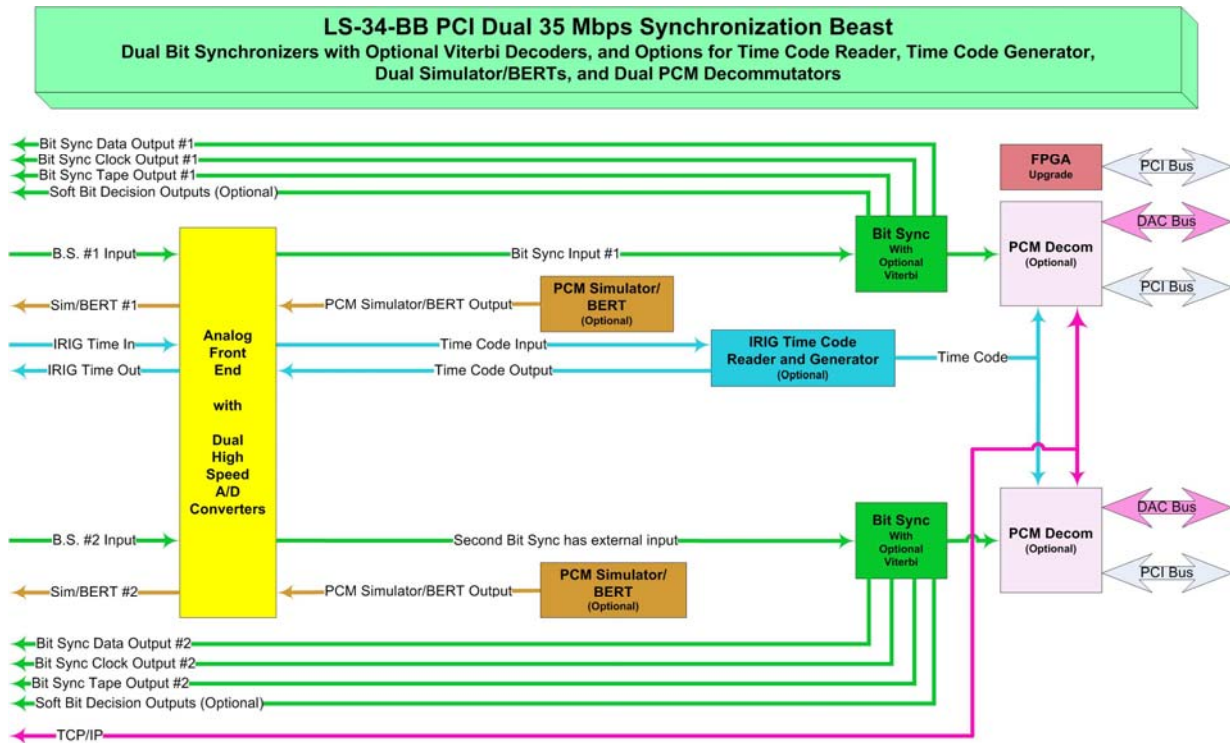
<http://www.lumi-star.com>

*Preliminary Data Sheet, specifications are subject to change.*

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### Ordering Information:

The following single and dual channel configurations are available. Firmware upgrades are available to increase the number of functions performed in FPGA.

Lumistar LS-34-B Single Channel Part Numbering				
Data Rate (Mbps)	Bit Sync	Bit Sync and Decom	Bit Sync with Viterbi	Bit Sync with Viterbi and Decom
10	LS-34-B-01	LS-34-B-11	LS-34-B-21	LS-34-B-31
20	LS-34-B-02	LS-34-B-12	LS-34-B-22	LS-34-B-32
35	LS-34-B-03	LS-34-B-13	LS-34-B-23	LS-34-B-33

Lumistar LS-34-BB Dual Channel Part Numbering				
Data Rate (Mbps)	Dual Bit Sync	Dual Bit Sync and Dual Decom	Dual Bit Sync with Viterbi	Dual Bit Sync with Viterbi and Dual Decom
10	LS-34-BB-51	LS-34-BB-61	LS-34-BB-71	LS-34-BB-81
20	LS-34-BB-52	LS-34-BB-62	LS-34-BB-72	LS-34-BB-82
35	LS-34-BB-53	LS-34-BB-63	LS-34-BB-73	LS-34-BB-83

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## LS-34-BB Synchronization BEAST PCI Board Dual 35 Mbps Bit Synchronizers and Dual Multifunction Decoms Data Sheet

### SPECIFICATIONS:

#### Bit Synchronizer Data Rates:

Bit Rate (NRZ codes) 100 bps to 10, 20, or 35 Mbps  
Bit Rate (Other codes) 100 bps to 5, 10, or 17.5 Mbps

#### Input Signal Characteristics:

Inputs per Bit Sync 2 SE or 1 Diff SW selectable  
Input Impedance: Factory set for 75 $\Omega$ ,  
50 $\Omega$ , 130  $\Omega$ , 1K $\Omega$  (jumper selectable)  
Auto-detect (normal or inverted)  
Input Polarity:  
Input Signal Amplitude: 0.5 V pp to 10 V pp  
Maximum Voltage Input: 5V RMS for 50 $\Omega$ , 75 $\Omega$ , 130 $\Omega$  Inputs  
10V RMS for 1K $\Omega$  Impedance  
Maximum DC Offset: +/- 5V for 50 $\Omega$ , 75 $\Omega$ , 130  $\Omega$  Inputs;  
+/- 10 V for 1K $\Omega$  Impedance  
Dynamic AC baseline: Baseline variations up to 100% of the  
input signal at rates to 0.1% of the signal  
frequency for sinewave or sawtooth  
signals (100 Hz max)

#### Phase-Locked Loop Performance:

Loop-Bandwidth: Programmable from 0.01% to 2% of the  
bit rate of the input signal.  
Acquisition Range: 4 to 8X selected Loop-Bandwidth  
Tracking Range: Up to 16X selected Loop-Bandwidth

#### Bit Sync Input & Tape Output Codes:

NRZ codes: NRZ-L, NRZ-M, NRZ-S  
RZ codes RZ  
Split phase codes BI $\phi$ -L, BI $\phi$ -M, BI $\phi$ -S  
Miller codes DM-M, DM-S, M<sup>2</sup>-M, M<sup>2</sup>-S  
Randomized codes RNRZ-L, RNRZ-M, RNRZ-S  
Randomization sequence: 2<sup>11</sup>-1, 2<sup>15</sup>-1, 2<sup>23</sup>-1

#### Bit Sync Output Signals:

Data TTL and RS-422 Driven  
Selectable Phase Clock TTL and RS-422 Driven  
Selectable for 0, 90, 180, 270 degrees  
Tape Outputs TTL and RS-422  
Lock Status In Status Register  
Signal Quality Status In Status Register

#### Viterbi Decoding:

Viterbi Decoding Rate 1/2, K=7  
BER Improvement 5.2 dB @ 10<sup>-5</sup> BER

#### Bit Error Rate Performance:

Bit error rate degradation from theory for Eb/No from 0dB to 10 dB will be less than the values below:

Bit Error Rate Degradation from Theory (preliminary data)	
Data Rate	Degradation
10 Kbps	<0.7 dB
1 Mbps	<0.5 dB
10 Mbps	<1 dB
20 Mbps	<1.5 dB
35 Mbps	<2.0 dB

#### Capture Threshold:

The Capture Threshold when the applied signal has a S/N ratio within 1 dB of the specified synchronization threshold, has a Gaussian white noise up to three times the bit rate, and has no jitter or base line variations on the input signal is defined below:

##### Codes:

NRZ  
BI $\phi$

##### Capture Threshold:

-1 dB (-3 dB typical)  
+1 dB (+0 dB typical)

#### Synchronization Hold:

The LS-40 Bit Synchronizer is capable of maintaining synchronization during periods of a signal loss or during continuous periods of 1s or 0s lasting up to 245 bits in every 1024 bits, for NRZ coded signals up to 5 Mbps or BI $\phi$  coded signals up to 2.5 Mbps, providing:

- S/N ratio is greater than 12 dB
- PLL bandwidth is equal to 0.1%
- 50% Transition Density when the signal is present
- Input signal has no jitter or base line variations
- Signal has a constant amplitude

#### Acquisition Time:

The mean acquisition time is a function of the Loop Bandwidth and will be less than 100 bits with a Loop Bandwidth of 1% and less than 150 bits with a Loop Bandwidth of 0.1% for NRZ signals up to 5 Mbps or BI $\phi$  signals up to 2.5 Mbps, providing:

- Gaussian white noise in a band up to three times the bit rate
- Transition Density is greater than 2% of the bit rate
- Signal has no jitter or baseline variations on the input signal

#### Convolutional Coding:

Convolutional Encoding Rate 1/2, K=7  
On PCM Simulator Outputs

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### PCM Decommutator:

Input Data Rate	64 bps to 35 Mbps
Input Signals	NRZ-L data & 0 degree clock
Input Levels	Single-ended TTL & RS-422
Word Length (VWL)	Variable from 3 to 16 bits per word on a word-by-word basis
CRC checker	CRC16/CCITT
Minor Frame Length	2 to 65,536 words per minor frame
Major Frame Length	Up to 1024 minor frames per major frame
Bit Order	MSB or LSB-first (word-by-word basis)
Frame Sync Pattern	Up to 64 bits (any pattern with don't care bits (X) may be used)
Frame Sync Location	Beginning or end of the frame
Frame Sync Strategy	Adaptive mode (search-lock-verify) & burst mode (search-lock)
Sync Error Tolerance	0 to 15 bits (selectable)
Sync Slip Window	1, 3, 5, 7 bits wide (selectable)
Data Polarity	Normal, inverted or automatic
Subframe Sync	FCC (FAC), SFID or URC (Optional)
URC Location	Any 64 bit window within the first minor frame not including the last bit in the minor frame
SFID Location	Any series of contiguous bits not including the last bit in the minor frame

### PCM Simulator:

Outputs	Data, 0 degree clock & minor frame strobes
Output Levels	Single-ended TTL & RS-422
Output Data Rate	64 bps to 35 Mbps (NRZ codes) 64 bps to 17.5 Mbps (all other codes)
PCM Codes	NRZ-L/M/S, BI $\phi$ -L/M/S DM-M/S, RNRZ-L ( $2^{11}-1$ , $2^{15}-1$ )
Word Length (VWL)	Variable from 3 to 16 bits per word on a word-by-word basis
CRC Generator	CRC16/CCITT
Minor Frame Length	2 to 16,383 words per minor frame
Major Frame Length	Up to 1024 minor frames per major frame
Bit Order	MSB or LSB-first on a word-by-word basis
Frame Sync Pattern	Fully programmable
Sub-Frame Sync	FCC (FAC), SFID & URC; URC Fully programmable
Common Words	May be a single value or selected from a group of one minor frame or 2048 words whichever is less.
Unique Words	Seven may be programmed in any mainframe, super-commutated, or subcommutated channel.
Waveform Words	Five may be programmed to appear in every frame at the same location.

### BERT:

Pseudo-random patterns	11, 15, 17, 19, 21, 23, and 25 bit
Bit Error Rate	Indicated on Software
Error Count	Indicated on Software
Forced Error Modes	Continuous Forced Error Single Bit Forced Error
History Log	Yes

### Pre-Modulation Filters

Single Channel Board	16 Selectable filters
Dual Channel Board	8 Channels for each Simulator

### Environmental:

Operating Temperature	0° to +50° C
Non-Operating Temp	-25° to +70° C
Operating Humidity	0 to 90% (Non-condensing)
Non-Operating Humidity	Protect from moisture and contamination

### IRIG A/B/G Reader/Generator:

Reader Input Format	IRIG A, B, or G
Time Reader Rate	½, 1, or 2 times normal rate
Input signal level	1V p-p nominal
Latency	2µsec (maximum)
Data Outputs	Automatic time tags for PCM data blocks (time accessible in register space)
Generator Output Format	IRIG A, B, or G
Time Generator Rate	½, 1, or 2 times normal rate

### Physical:

Form Factor	Full length PCI mainboard SBC height With Analog Front End daughterboard
Power Requirements	2.2 A @ 3.3 Volts (typ) 200 mA @ +5 Volts (typ) 750 mA @ +12 Volts (typ) 400 mA @ -12 Volts (typ)