



# LS-040 Series User's Manual

## Programmable Digital PCM Bit Synchronizer

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## 1. Introduction

### 1.1 General

This document is the User's Manual for the Lumistar LS-040 Series Programmable Digital PCM Bit Synchronizer. The intent of this document is to provide physical, functional, and operational information for the end user.

The LS-040 Series Programmable Digital PCM Bit Synchronizer provides correlated clock and data recovery from an incoming PCM stream. The LS-040 provides translation of various PCM formats and provides a user programmable PCM output format, which may be used for tape storage or as a means of providing PCM format translation. The programming range of the LS-040 is from 50bps to 20Mbps for NRZ PCM codes and 50bps to 10Mbps for all other support PCM codes.

The LS-040 mechanical format is that of a custom mezzanine board. This format is compatible with a number of products manufactured by Lumistar including the LS-050 decommutator cards and the LS-22 series IF receiver cards. The LS-040 is also compatible with several boards manufactured by SBS Technologies Inc. The LS-040 card was designed to be a drop-in replacement for the SBS model 4400-TF Analog Bit Synchronizer. Thus, the LS-040 can be functionally mounted and controlled by SBS model 4422-series products. In addition, the LS-040 board may be used in a stand-alone role by using its auxiliary power and control interfaces.

Table 1-1 below provides specifications for electrical, mechanical, and operational characteristics of the LS-040 Programmable Digital PCM Bit Synchronizer. A block diagram of the LS-040 is shown in Figure 1-1.

### 1.2 Manual Format

This manual is separated into the following sections:

- Chapter 1 provides a brief product overview and technical specifications
- Chapter 2 provides LS-040 theory of operation
- Chapter 3 provides installation and configuration instructions
- Chapter 4 provides programming information

Category:	Specifications:	Details:
<b>Mechanical</b>		
	Envelope Dimensions	6.65"(L) x 2.85"(W) x 0.55" (H)
	Form Factor	Custom Mezzanine; Stand-alone
	Weight	< 5oz.
<b>Electrical</b>		
	Individual power requirements	+5VDC @ 850mA
		+12VDC @ 10.7mA
		-12VDC @ 208mA
	Total Power	< 6.9W
<b>Inputs</b>		
	Quantity	1 SE/Differential Input; Jumper Selected
	Impedance	50, 75 or 1K $\Omega$ ; Jumper Selectable
	Rates (Option dependent)	50-20Mbps NRZ Codes; 50-10Mbps others
	Polarity	Normal or Inverse; Software Programmable
	Signal Amplitude	0.1V to 10V p-p
	Maximum Voltage permissible	25V RMS
	Loop Bandwidth (LBW) settings	0.01 to 2% (data rate dependent)
	Acquisition Range	+/- (4 x LBW Setting)
	Tracking Range	+/- (10 x LBW Setting)
	Mean Acquisition Time	100-150 bits
	Discrettes	(3) TTL; <i>Consult factory for use</i>
<b>Outputs</b>		
	NRZ-L Data Output	+TTL, -TTL
	0° Clock Output	+TTL, -TTL
	PCM Output	1V p-p @ 50 $\Omega$ ; Programmable Line Codes
	PCM PRN Output	+TTL, -TTL; Programmable Line Codes
	PCM PRN Patterns	2 <sup>11</sup> -1, 2 <sup>15</sup> -1; Programmable
<b>Control/Status</b>		
	Parallel Command Interface	Standard PC Parallel Interface
	Serial Control/Status Interface	RS-232C Interface; Selectable BAUD rate
<b>PCM Line Codes</b>		
	Non-return to Zero Codes	NRZ-L, NRZ-M, NRZ-S
	Bi-Phase Codes	Bi $\Phi$ -L, Bi $\Phi$ -M Bi $\Phi$ -S
	Delay Modulation (Miller) Codes	DM-M, DM-S, M <sup>2</sup> M, M <sup>2</sup> S
	Return to Zero Codes	RZ
	Randomized Codes	RNRZ-L, RNRZ-S, RNRZ-M
	Randomizing Sequences	2 <sup>11</sup> -1, 2 <sup>15</sup> -1, 2 <sup>17</sup> -1, 2 <sup>23</sup> -1
<b>Environmental</b>		
	Temperature, Operational	0° to 70° C (Commercial)
	Temperature, Storage	-20° to 70° C
	Humidity, non-condensing	<40° C 0-90%, >40° C 0 to 75%

**Table 1-1 Specifications for the LS-040 Series Digital Bit Synchronizer**

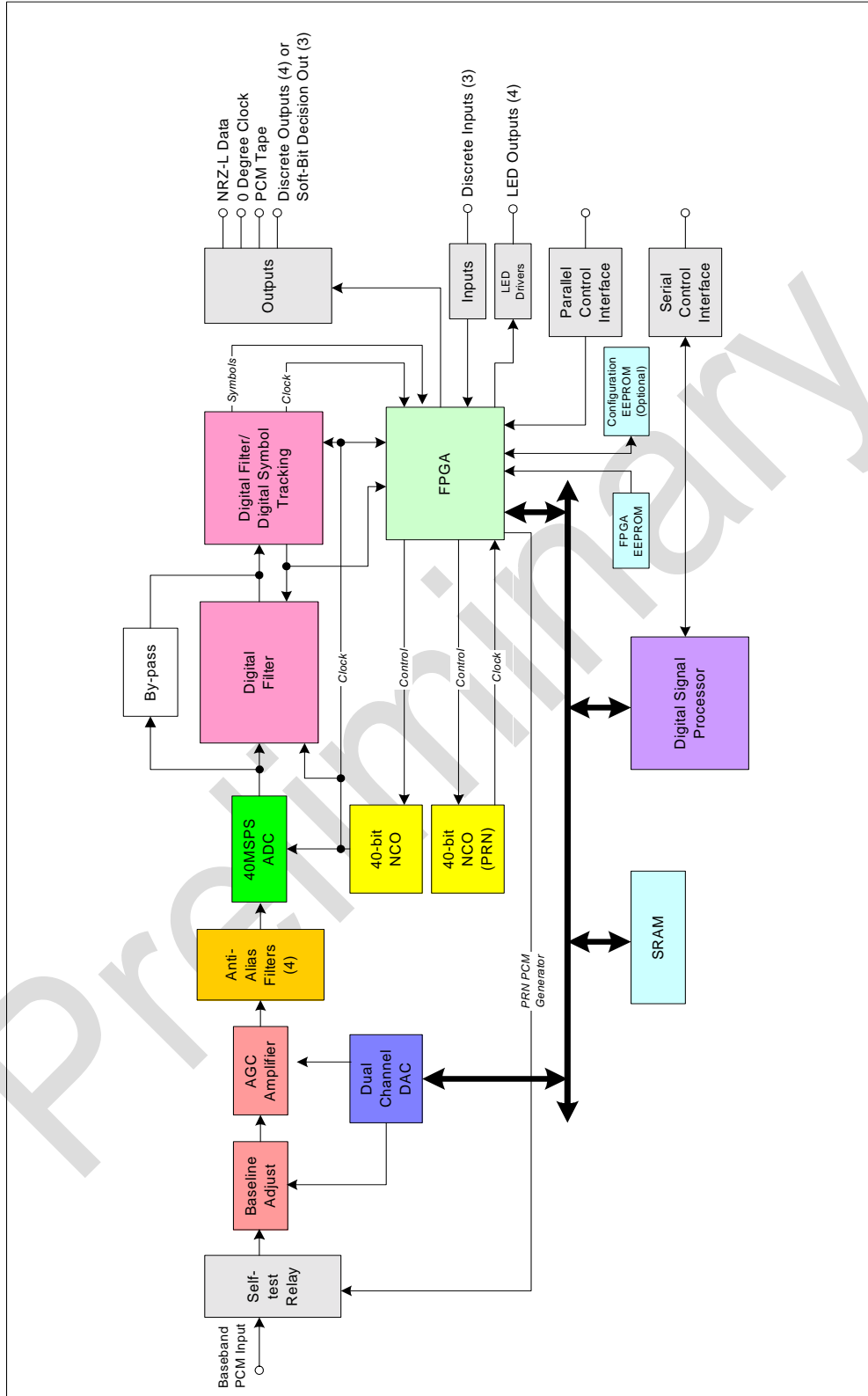


Figure 1-1 Block Diagram of the LS-040 Series Digital Bit Synchronizer

## 2. Theory of Operation

In order to more clearly understand the operation of the LS-040 Digital Bit Synchronizer, it is important to examine the general functionality and use of a bit synchronizer. The primary function of any bit synchronizer is the following:

- Receive an analog Pulse Code Modulated (PCM) input data stream
- Adjust the incoming data stream for various signal levels and offsets
- Filter unwanted frequencies and noise from the primary bands of interest
- Process the data stream to recover the incoming data with a correlated clock
- Provide the correlated clock and data output for further data processing and/or data storage

The LS-040 provides all of these functions via digital control and processing utilizing various Digital Signal Processing (DSP) technologies. This architecture provides for greater signal integrity and control and reduced operational temperature sensitivity while utilizing far less power than a traditional analog bit synchronizer. Since the LS-040 contains no analog data filters, variations in performance from one unit to the next are nearly eliminated.

For the following sections, refer to the block diagram of Figure 1-1 for additional details.

### 2.1 Input Section

The input section of the LS-040 Digital Bit synchronizer is composed of the following: a self-test input section relay, an input termination impedance selection, digital feed-back Automatic Gain Control (AGC) circuitry, a bank of four fixed anti-alias filters, and a digital feed-back Baseline restoration adjustment circuit.

The self-test input relay is used in conjunction with the Built-In-Test (BIT) provisions of the unit to provide switching of the on-board PRN generator test signals to the input section for power-up functional tests.

The input termination is provided for proper impedance matching to the PCM source. Three termination impedances are provided: 50 $\Omega$  ohms, 75 $\Omega$  ohms, and 1K $\Omega$ . In addition to these typical termination impedances, additional custom termination impedances can be provided. Consult the factory for availability.

The initial stage of the input section is a digitally controlled Baseline restoration circuit. The incoming PCM stream may be DC or AC coupled. The front end of the LS-040 blocks the DC components of the incoming stream and AC couples the signal. Slight variations due to "baseline gallop" may still interfere with the proper processing of the PCM signal. To compensate, the DSP processing engine feeds digital correction factors back to the baseline restoration circuit.

Automatic Gain Control adjusts the input signal to the proper processing levels. The incoming signal may vary between 100mVp-p and 10Vp-p. The maximum input signal permissible without damage is 25V p-p. A 10-bit Digital-to-Analog Converter (DAC) channel controls the AGC circuit. Data is fed to the DAC via the Digital Signal Processing engine. This process constantly monitors the incoming signal for variations in amplitude and adjusts the signal to the AGC amplifier accordingly.

The signal is then passed through a bank of four fixed low-pass anti-alias filters. The anti-alias filters are used to eliminate interfering signals caused by the digital processes of the LS-040.

Processes of digital decimation and interpolation used by the DSP engines on the LS-040 generate digital “disturbers” that can fall within the bands of interest. The anti-alias filters block these unwanted by-products from interfering with the input signals.

## **2.2 Digital Filtering and Processing**

Once the PCM input signal has been gain and baseline compensated by front end processing, a high-performance Analog-to-Digital Converter (ADC) is used to digitize the PCM input stream. Data is then sent through a series of digital decimation/interpolation data filtering elements followed by a digital symbol tracker. Symbol and clock information is further processed by a Field Programmable Gate Array (FPGA) to convert and decode the input PCM format.

The clock sources for the processing engine and the PRN test generator are provided via two individually controlled 40-bit Numerical Controlled Oscillators (NCOs). The two NCOs use a common precision crystal oscillator as a reference source to minimize overall jitter and drift.

## **2.3 Control, Sequencing and Memory**

At the core of the LS-040 architecture is a 30 million-instruction-per-second Digital Signal Processor and a Field Programmable Gate Array (FPGA). The FPGA provides hardware control logic required by the LS-040 architecture. The dedicated processor is used for overall software control and sequencing of the bit synchronizer DSP engines, direction and control of the user interfaces, as well as an interface to system memory components.

Memory on the LS-040 is composed of the following: SRAM, internal DSP FLASH memory, an FPGA configuration EEPROM, and a serial configuration EEPROM,. The processor stores the executable code of the LS-040 in its internal FLASH memory. This memory is non-volatile and is **not** accessible to the user. This memory is not programmed during use and contains no operational parameter storage. SRAM is used for data variable memory storage during LS-040 operation. This memory is volatile and is cleared upon loss of power. The FPGA is loaded at power-up via a serial EEPROM. This EEPROM is non-volatile and is **not** accessible to the user. The LS-040 contains a serial EEPROM that stores the last valid configuration information of the LS-040 such as bit rates, PCM processing codes, loop-bandwidth settings, etc. This memory is non-volatile and is automatically configured by the user writing setup information to the bit sync. The configuration EEPROM may be optionally removed by the customer for security related concerns. To remove the configuration EEPROM functionality, simply remove the 93CS66 EEPROM (U9) from its socket near the JP1 header (reference Figure 3-1).

If the configuration EEPROM is removed, the LS-040 will continue to operate normally. However, at the initialization of power to the unit, the LS-040 will always default to a PCM input format of NRZ-L at a data rate of 200Kbps.

## **2.4 User Control and Status Interfaces**

The LS-040 can be controlled via two interface channels. User's can control and status the LS-040 via a bi-directional IEEE 1284 PC parallel interface bus or via the EIA-232 (commonly

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referred to as RS-232) serial interface bus. Consult section 4 of this manual for additional details of each of the interfaces.

## 2.5 PCM Link Analysis Functions (optional)

The LS-040 provides an optional Link Analysis function. This function allows the on-board PRN generator to be output to an external PCM processing link that the user wishes to performance test. This PCM output can be programmed to be any of the supported LS-040 formats. The PRN pattern generator can be programmed for a pseudo-random pattern length of  $2^{11}-1$  (2,047 bits) or  $2^{15}-1$  (32,767) bits. This output can then be transmitted through the desired PCM processing link.

The returned PCM stream is then input to the LS-040 input where the internal processing utilizes a sliding-correlator to count Bit Errors and calculate Bit Error Rate (BER) performance from the external PCM link. This function is useful in determining link integrity and overall performance. Figure 2-1 below shows the interconnection of this test setup.

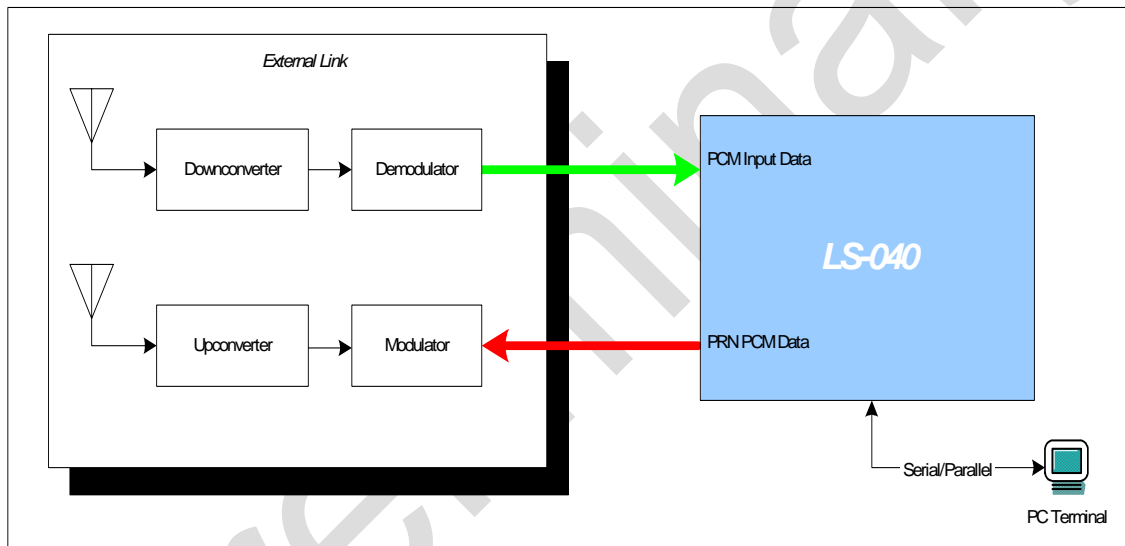


Figure 2-1 PCM Link Analysis using the LS-040 Series Digital Bit Synchronizer

### 3. Installation and Configuration

Chapter 3 provides installation and configuration information. This chapter will help locate serial numbers and product configuration information, familiarize the user with the layout of the board, and properly set up the hardware.

#### 3.1 Product Identification

The LS-040 contains a number of configuration jumpers and a configuration switch to control various functions of the LS-040. Figure 3-1 contains a diagram of the top and bottom sides of the LS-040 with indications of jumper and switch locations.

The LS-040 model number, serial number, revision information, and product options are denoted on the rear of the board under the Lumistar LLC name. Figure 3-1 depicts the location of these configuration details. Consult the product data sheet for additional option configurations.

#### 3.2 Hardware Configuration

The LS-040 contains a number of configuration jumpers and a configuration switch to control various functions of the LS-040. Figure 3-1 contains a diagram of the top and bottom sides of the LS-040 with indications of jumper and switch locations.



**Warning:** The LS-040 contains several jumpers that are configured during factory test. Jumpers other than those depicted in Figure 3-1 should not be altered for proper operation of the unit.

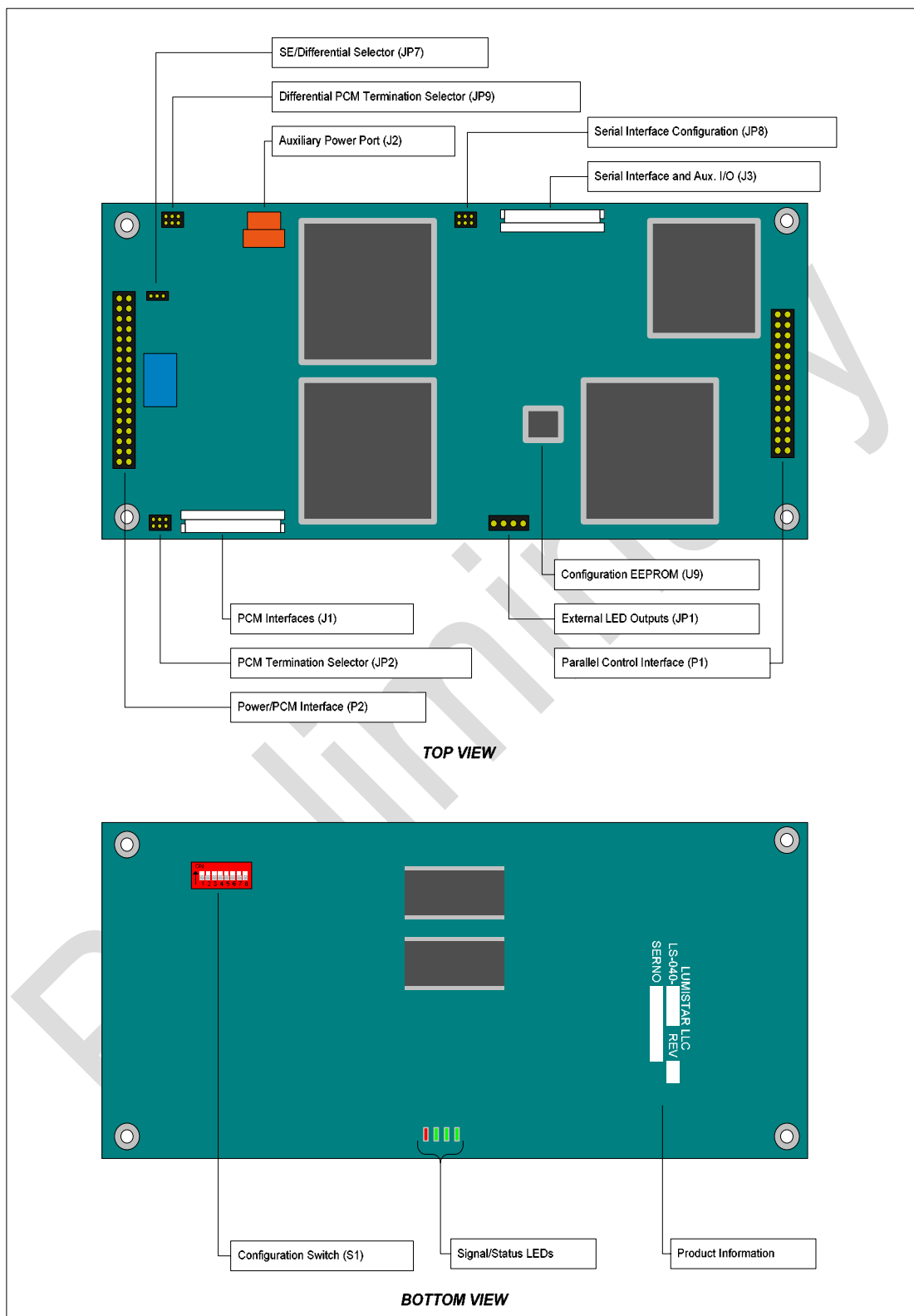


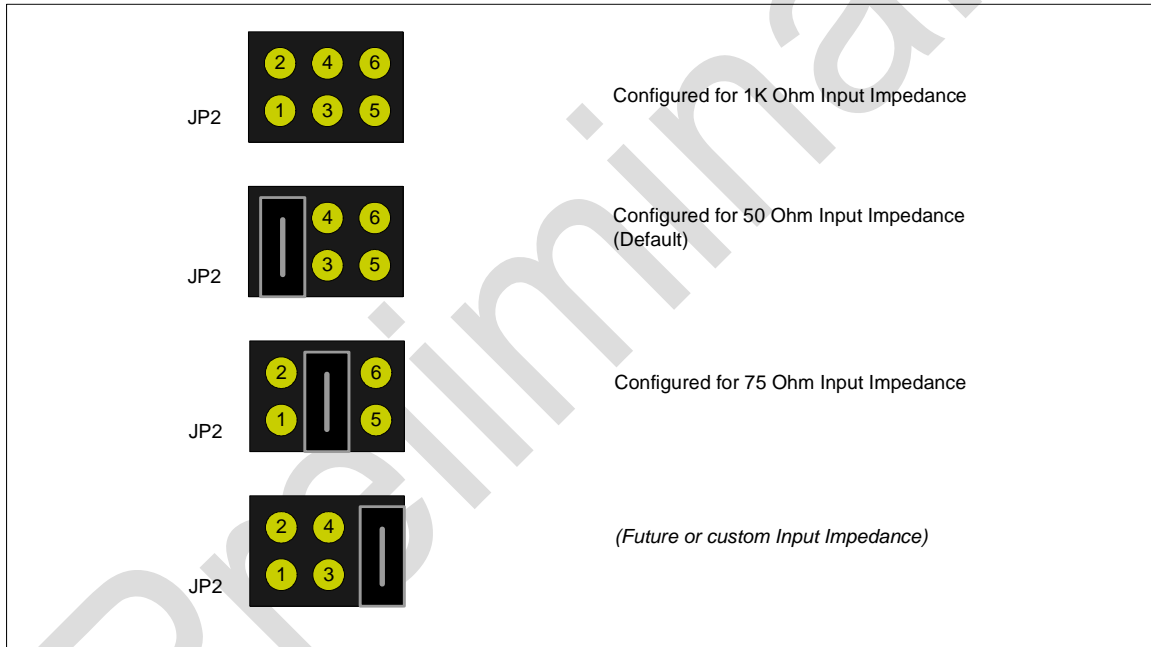
Figure 3-1 LS-040 Configuration jumpers/switch locations

All jumpers on the LS-040 are arranged with the reference designators silk-screened near the pin 1 location

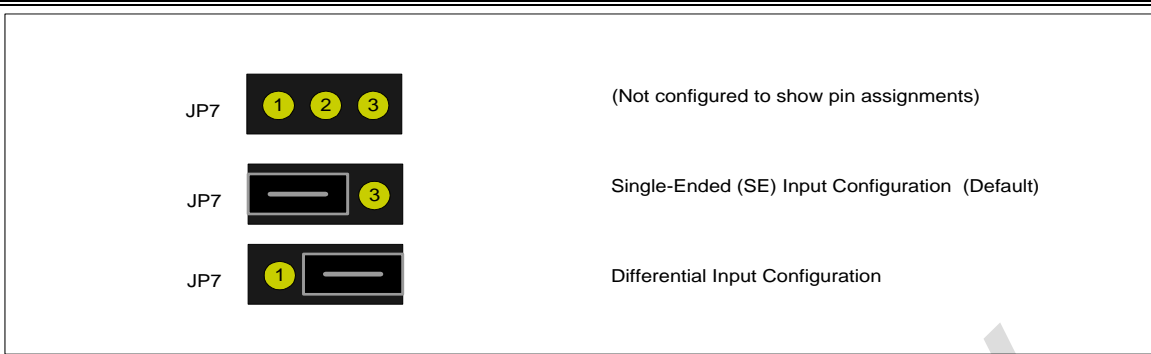
The LS-040 is shipped with its jumpers in the configuration shown in Table 3-1. Configuration details for these jumpers are given in Figures 3-2 through 3-5.

Jumper	Designation	Configuration Default	Jumper(s) Configuration	Reference Figure
JP2	PCM Termination	50 Ohm Input	JP2 1-2	3-2
JP7	SE/Differential Input	SE Input	JP7 1-2	3-3
JP8	Serial TX/RX Configuration	J3-12(TX) J3-14(RX)	JP8 2-4/JP8 3-5	3-4
JP9	Differential Termination	100 Ohm Input	JP9 1-2/ JP9 3-4	3-5

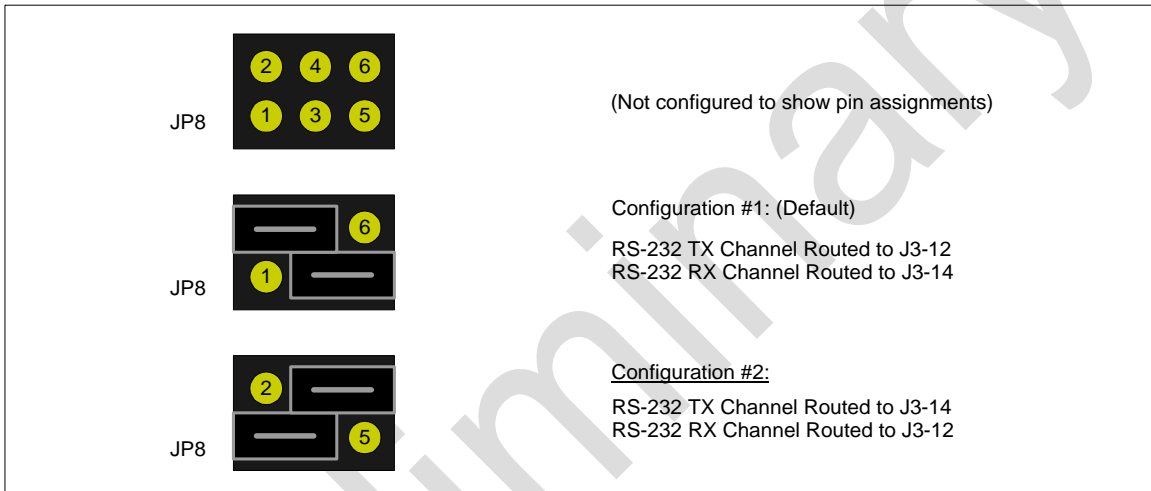
**Table 3-1 LS-040 Default Jumper Configurations**



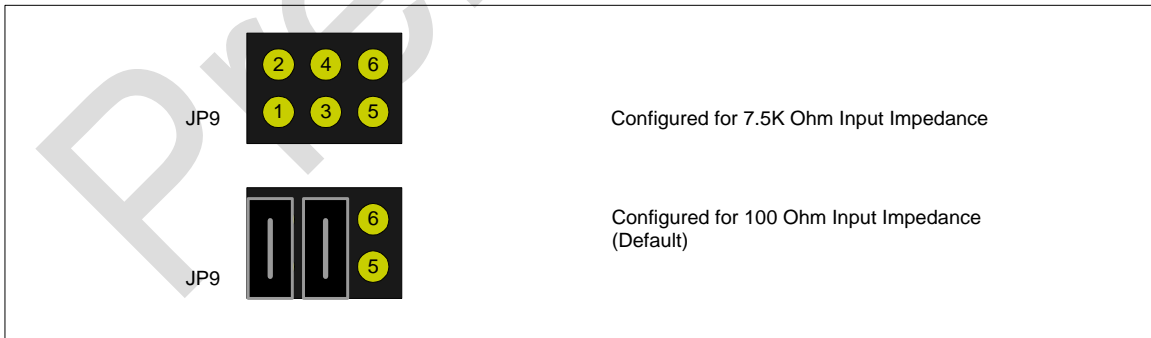
**Figure 3-2 LS-040 Single-Ended (SE) Input Termination Configuration Jumpers**



**Figure 3-3 LS-040 Single-Ended (SE) versus Differential Input Selector Jumper**



**Figure 3-4 LS-040 Serial TX/RX Configuration Jumpers**




**Figure 3-5 LS-040 Differential Termination Configuration Jumpers**

The LS-040 also provides additional configuration options via a switch on the rear side of the board as shown in Figure 3-1. Switch S1 functions are detailed in Figure 3-6.

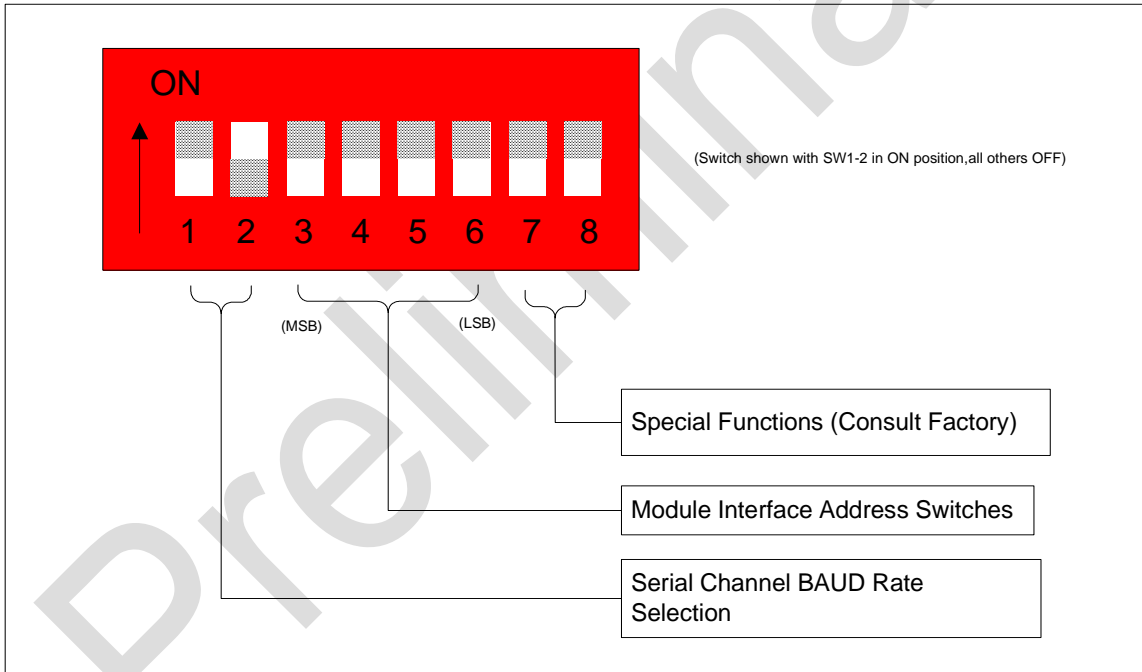
Switch S1 special function switches (S1-7 and 8) are for future functionality and MUST remain in the OFF position.

The module address switches (S1-3 through S1-6) are used to configure the serial and parallel interface operation for instances where more than one module is being commanded via the given command bus controller. The address function is binary in nature ranging from 0x0 (0) to address 0xF (15). The OFF position assigns a module address of "0". The ON position provides a module address of "1". See section 4 of this manual for further details on the operation of this switch position.



**Warning:** If the LS-040 is being commanded as the only unit of an independent controller, S1-3 through S1-6 must remain in the OFF position (address 0x0) for proper operation.

Switch S1-1 and S1-2 are used to set the serial channel BAUD rate. Table 3-2 indicates the BAUD rate selected by different switch settings.



**Figure 3-6 LS-040 Configuration Switch (S1)**

Switch S1-1	Switch S1-2	Serial BAUD Rate
OFF	OFF	4800 bps
OFF	ON	9600 bps
ON	OFF	19200 bps
ON	ON	38400 bps

**Table 3-2 LS-040 Serial Interface BAUD Rate Selection switches**

### 3.3 Physical Installation

The LS-040 mechanical and interface design provides for it being directly interfaced to the following products:

- Lumistar Model LS-050 Decommutator/Simulator
- Lumistar Model LS-022 70MHz Receiver
- Lumistar Model LS-042 Bit Synchronizer Carrier Card
- Lumistar Model LS-022 70 MHz Receiver/Spectral Display Unit
- SBS Model 4422-V64 VME Decommutator/Simulator
- SBS Model 4422-PCI PCI Decommutator/Simulator

To install the LS-040, the following procedure should be followed:

1. Perform normal system shutdown of the PC system and remove the primary power plug.
2. Obtain the unit on which the LS-040 is to be mounted.
3. Orient the LS-040 with the P1 and P2 mounting connectors positioned over the mating connectors. The mounting holes at the corners of the LS-040 should align with the stand-offs used for securing the device.
4. Install the mounting screws at the corners of the device to secure the unit.



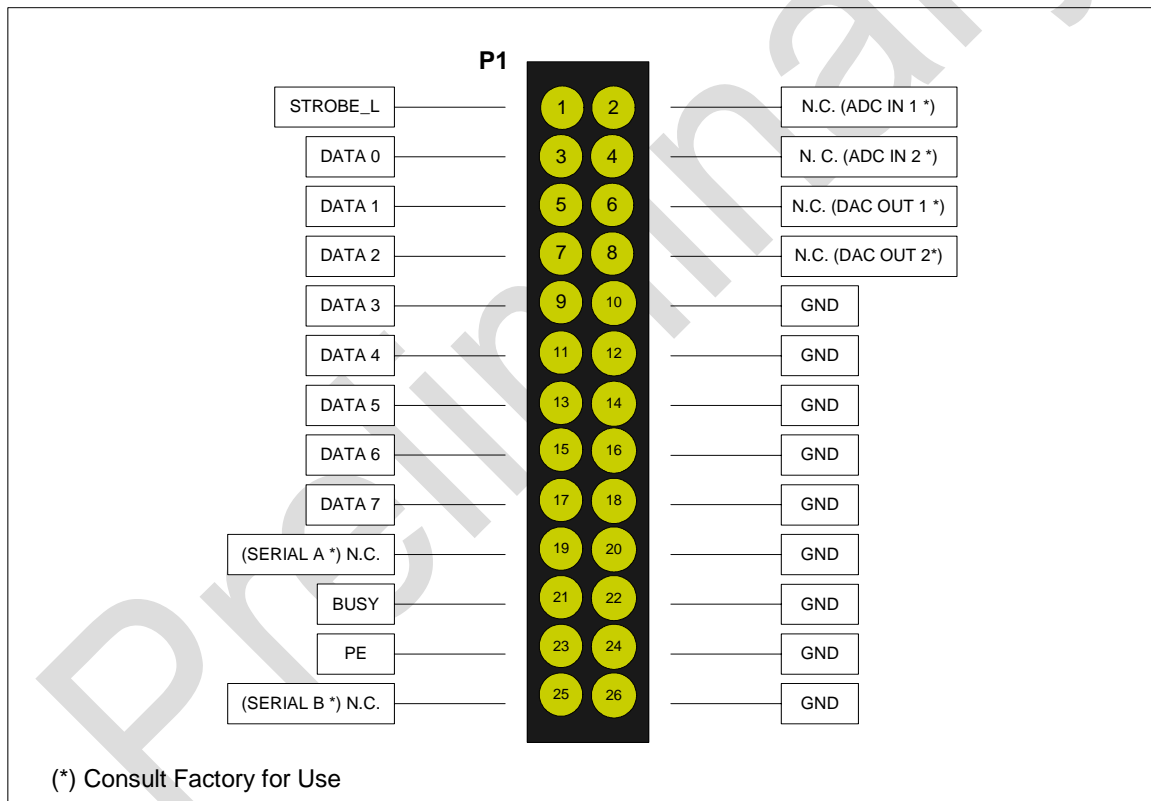
**Warning:** The interface pins of the LS-040 are fragile. Insure that the interface connectors are properly aligned prior to installation to prevent pin fractures.

### 3.4 Interconnection

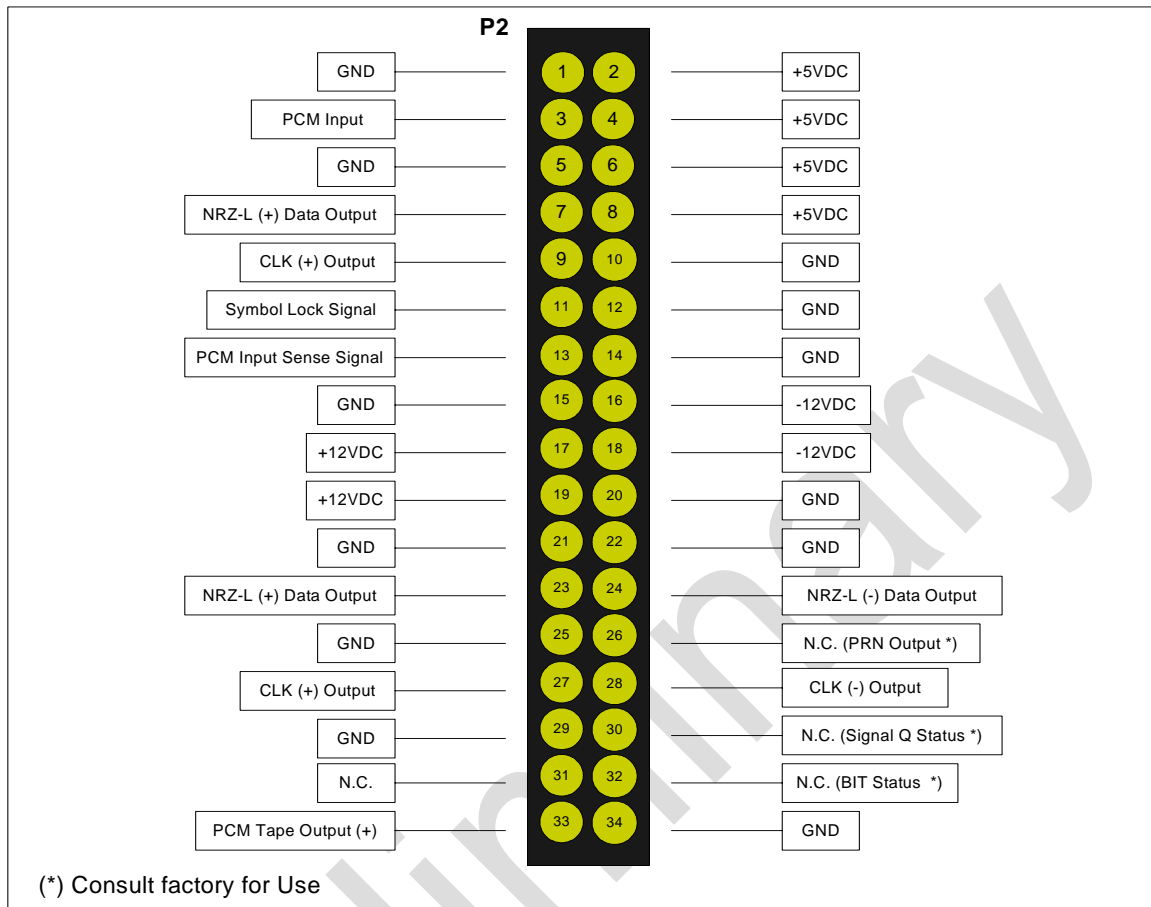
The LS-040 provides six user interface connectors. In the standard configuration, only the P1 and P2 connectors are required for interfacing the LS-040 to its intended host. For additional functionality, and for stand-alone operation, four additional interface connectors are provided. Table 3-3 provides mating connector information for mating with all interface connectors of the LS-040. Figures 3-7 and 3-8 provide interface pin-outs for the P1 and P2 connectors. Tables 3-4 and 3-5 provide pin-out details for the auxiliary PCM interface connector J1 and serial auxiliary connector J3 respectively. Table 3-6 provides pin-out information for the stand-alone auxiliary power connector J2. Figure 3-9 provides pin-out information for the auxiliary external status LED output connector JP1 and the status LED definitions.

Connector	Function	Mating Connector Part No.	Manufacturer
P1 (0.018 Pins)	Command Bus Interface	SD-113-G-2	Samtec
P1 (0.025 Pins)	Command Bus Interface	SSW-113-01-G-D	Samtec
P2 (0.018 Pins)	PCM and Power Interface	SD-117-G-2	Samtec
P2 (0.025 Pins)	PCM and Power Interface	SSW-117-01-G-D	Samtec
J1	PCM Interface Connector	51146-1400	Molex
J2	Auxiliary Power Connector	22-01-2047	Molex
J3	Serial/Auxiliary	51146-1400	Molex
-	Terminals, J1/J3 Connector	50641-8141	Molex
-	Terminals, J2 Connector	08-50-0114	Molex
-	Crimp tool for J1/J3 Term.	57352-5000	Molex

**Table 3-3 LS-040 Mating Connectors**



**Figure 3-7 LS-040 (P1) Parallel Interface Control Connector**



**Figure 3-8 LS-040 (P2) PCM and Power Connector**

<i>Pin Number</i>	<i>Function</i>
J1-1	PCM Input (+)
J1-2	PCM Input (-)
J1-3	Ground
J1-4	Clock Out (+)
J1-5	Clock Out (-)
J1-6	Ground
J1-7	NRZ-L Data Out (+)
J1-8	NRZ-L Data Out (-)
J1-9	Ground
J1-10	PCM Encoder Output (+)
J1-11	PCM Encoder Output (-)
J1-12	Ground
J1-13	PRN PCM Generator Output (+)
J1-14	PRN PCM Generator Output (-)

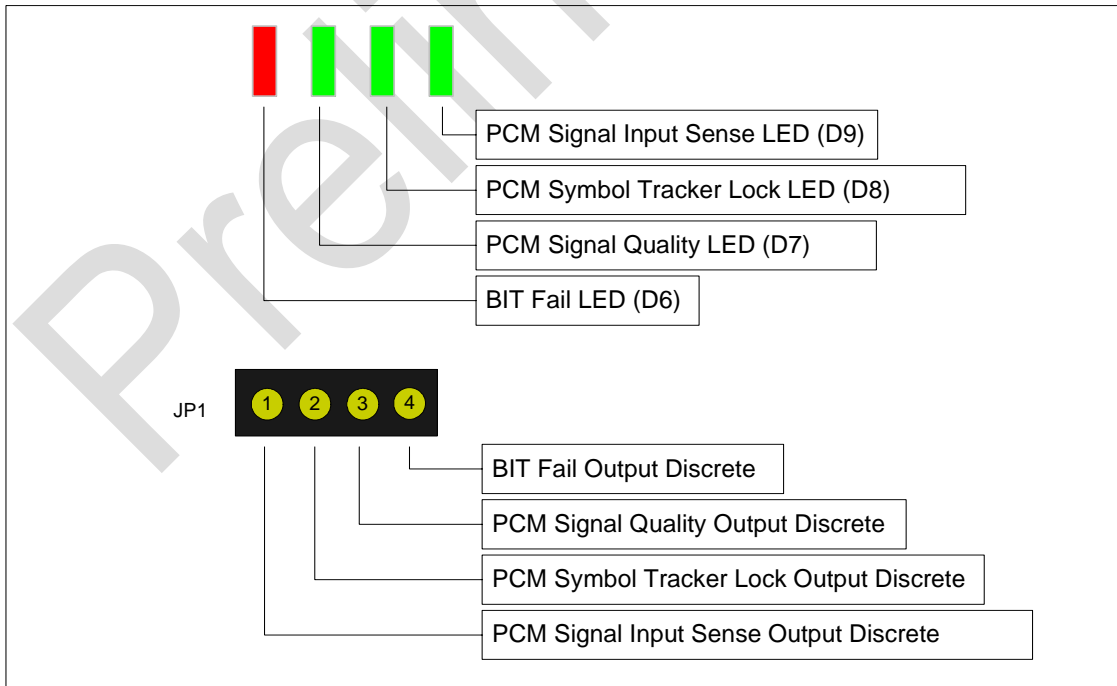
**Table 3-4 LS-040 Auxiliary PCM Interface Connector Pin-out**

Pin Number	Function
J3-1	Special Function Input 1
J3-2	Ground
J3-3	Special Function Input 2
J3-4	Ground
J3-5	Special Function Input 3
J3-6	Special Function Output 1 / Soft Decision D0
J3-7	Ground
J3-8	Special Function Output 2 / Soft Decision D1
J3-9	Special Function Output 3 / Soft Decision D2
J3-10	Ground
J3-11	Special Function Output 4
J3-12	Serial Interface A
J3-13	Ground
J3-14	Serial Interface B

**Table 3-5 LS-040 Auxiliary I/O Interface Connector Pin-out**

Pin Number	Function
J2-1	+12VDC
J2-2	+5VDC
J2-3	Ground
J2-4	-12VDC

**Table 3-6 LS-040 Auxiliary Power Connector Pin-out**



**Figure 3-9 LS-040 Auxiliary LED Interface and LED Definitions**

## 4. Programming

This chapter provides LS-040 programming and setup information. The LS-040 provides control and status interfaces via two hardware formats: an IEEE 1284 bi-directional PC parallel interface, and an EIA-232 (commonly referred to as RS-232) serial interface. Both interfaces utilize the same command formatting and command set. Provisions for programming multiple devices with one host interface will also be described in the following paragraphs.

### 4.1 Interface Command Set

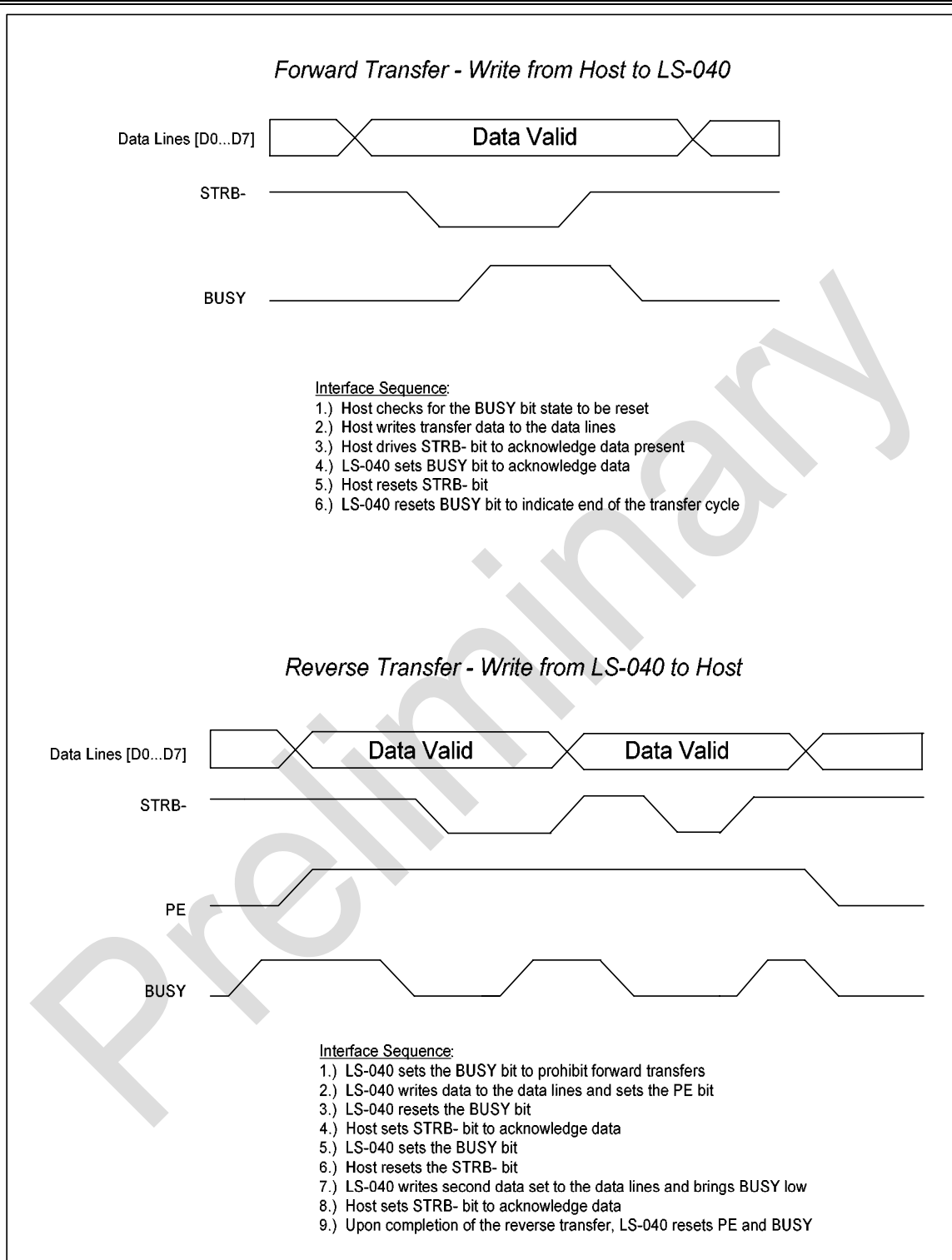
The LS-040 can be **commanded** via a standard PC bus interface or via the native mezzanine interfaces of the following devices: Lumistar LS-050 or LS-022 series products, or the SBS 4422 series products. In addition, a standard PC bus architecture or the host interfaces of the Lumistar LS-050 or LS-022 series products can be used to obtain operational **status** from the LS-040. The interface command set maintains compatibility with the existing interface definitions for the SBS 4400-series command set and makes some additions to the set to allow for additional features of the LS-040. A few of the existing commands have been redefined or are not applicable to the LS-040 design. Table 4-1 provides commands definitions for both the LS-040 and the corresponding commands for the SBS 4400-TF series interface. Paragraphs in section 4.2 of this document provide further detail of command definitions.

Commands (Hex)	Command Category	Lumistar LS-040 Function	Reference Section
0x0_	Control	General Operational Setup Commands	4.2.1
0x9_	Control	PCM Bit Rate Commands (x10 Mbps) [0..2 range]	4.2.2
0x1_	Control	PCM Bit Rate Commands (x1 Mbps) [0..9 range]	4.2.2
0x2_	Control	PCM Bit Rate Commands (x100kbps) [0..9 range]	4.2.2
0x3_	Control	PCM Bit Rate Commands (x10kbps) [0..9 range]	4.2.2
0x4_	Control	PCM Bit Rate Commands (x1kbps) [0..9 range]	4.2.2
0x5_	Control	PCM Bit Rate Commands (x100bps) [0..9 range]	4.2.2
0x6_	Control	PCM Bit Rate Commands (x10bps) [0..9 range]	4.2.2
0x7_	Control	PCM Bit Rate Commands (x1bps) [0..9 range]	4.2.2
0x8_	Control	Tentative Loop Bandwidth Commands	4.2.3
0xA_	Control	PCM Input Code Commands	4.2.4
0xB_	Control	PCM Output Code Commands	4.2.5
0xC_	Control	Auxiliary Commands	4.2.6
0xD_	Control	Auxiliary PCM Code Commands	4.2.7
0xE_	Status	Status Commands	4.2.8
0xF_	Address	Module Addressing Commands	4.2.9

Table 4-1 LS-040 Interface Command Set

#### 4.1.1 Command Formats

The LS-040 provides a bi-directional “master-slave” command and status interface. The IEEE 1284 parallel interface bus allows half-duplex interface flow. Flow control is maintained by the use of a “handshake” back to the commanding host via the BUSY discrete (See Figure 3-7, pin 22). The host **MUST** wait until the BUSY bit is returned low prior to issuing additional commands to prevent commands from being missed. Figure 4-1 illustrates the sequence of signal events that occur in both forward and reverse transmissions between the LS-040 and the host.



**Figure 4-1 LS-040 IEEE 1284 Bi-directional Interface Command Signal Sequences**

When utilizing the EIA-232 standard interface, the LS-040 monitors all asynchronously transmitted traffic from the commanding host without the use of a handshake signal. The serial interface can work in a full-duplex fashion. Command responses are transmitted back to the host via the alternate half of the serial signal path from the LS-040 to the host. Commands from the host are provided a higher priority than that of the status responses from the LS-040 when utilizing the serial interface bus.

The LS-040 decodes and processes commands via either bus interface and responds in accordance to the command set described in Table 4-1. Commands may be transmitted individually or in a group. In order to activate a particular command, or group of commands, the "*Master Configuration*" command (0x0A) must be transmitted as the last command in the sequence. The "*Master Configuration*" command tells the LS-040 internal software to gather up all changes that it received since its last update and apply them. If status commands are received from the host, a status response is transmitted. Figure 4-2 depicts the command set sequencing and responses from the LS-040.

Each command sent to the LS-040 is 1byte (8-bits) in length. Status responses are provided to status commands in 1-byte packets. A particular status command may result in multiple status bytes being returned via the reverse transfer channel.

If multiple LS-040's are being addressed by a single host, the host must maintain command and status sequencing. The host must maintain a command sequence which includes status commands with an individual terminal until the sequence is completed. Broadcast commands are prohibited.

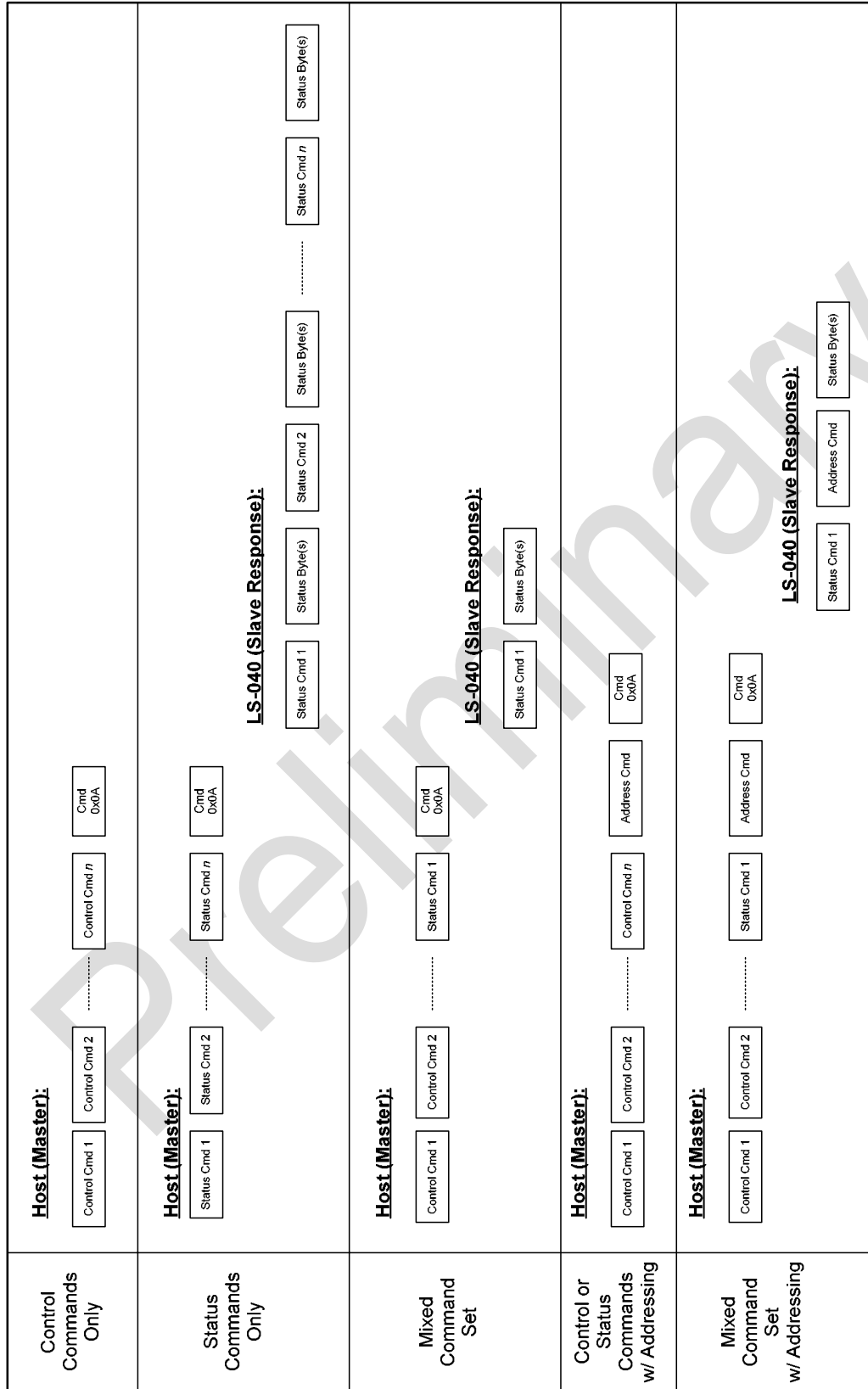


Figure 4-2 LS-040 Command Sequencing

### 4.1.2 Invalid, Undefined or Reserved Parallel Command Processing

The LS-040 has a defined set of commands for which it will respond. Commands may inadvertently be sent which are undefined or invalid. If this should occur, the LS-040 will ignore these commands and continue with the processing of additional commands.

### 4.1.3 Configuration EEPROM Storage

The LS-040 contains a configuration EEPROM (unless removed by the user) to store the last valid setup of the bit synchronizer variables. This is particularly useful for stand-alone operation where the unit needs to power-up in its last known configuration.

If the configuration EEPROM is installed, the last valid LS-040 setup will automatically be loaded at power-up. While in operation, any changes to the LS-040 operational setup will automatically be stored in EEPROM.

## 4.2 Command Details

The following sections detail the individual commands, status responses and their associated functions.

### 4.2.1 General Operational Setup Commands (0X0\_)

The LS-040 provides a set of general operational setup commands that maintain that enable and disable the main operating functions for the device. Table 4-2 lists these commands and their associated reference paragraphs that define the commands in greater detail.

General Setup Commands (Hex)	Function	Reference Section
0x00	(Undefined)	
0X01	(Undefined)	
0X02	(Undefined)	
0x03	(Undefined)	
0X04	(Undefined)	
0X05	(Undefined)	
0x06	(Undefined)	
0x07	(Undefined)	
0x08	Enable RRC Filtering	4.2.1.1
0x09	Enable I&D Bit Decision Methods	4.2.1.1
0x0A	Master Configuration Command	4.2.1.2
0x0B	(Undefined)	
0x0C	(Undefined)	
0x0D	(Undefined)	
0x0E	(Undefined)	
0x0F	(Undefined)	

**Table 4-2 LS-040 General Operational Commands**

#### 4.2.1.1 I&D and RRC Commands (0x08 and 0x09)

The LS-040 normally operates in an Integrate and Dump (I&D) mode during typical operations. This can be command using the “Enable I&D Bit Decision Method” command (0x09). If more rounded data is expected, an addition Raised-Root Cosine (RRC) filter can be applied to the data by commanding the “Enable RRC Filtering” command (0x08). This is commonly referred to as the “Filter Sample” method. In most operational environments, invoking the RRC filter option is not necessary.

These two commands are mutually exclusive. Only one of these commands is active at a given time. Either the LS-040 is operating in an I&D mode without the use of the RRC filter, or the LS-040 is operating in an I&D modes with the RRC filter enabled.

#### 4.2.1.2 Master Configuration Command (0x0A)

The “Master Configuration Command” (0x0A) is used by the LS-040 to indicate that a command sequence is complete and to act on the commands that it has received. The commanding host MUST issue this command at the end of a command sequence to signify the end of a command sequence and to initiate the desired changes.

#### 4.2.2 PCM Bit Rates Commands (0x1\_ through 0x7\_ and 0x9\_)

The LS-040 10Mbps model is capable of processing NRZ PCM inputs from 50bps to 10Mbps (50bps to 5Mbps all other formats) and the LS-040 20Mbps model is capable of processing NRZ PCM inputs from 50bps to 20Mbps (50bps to 10Mbps in all other PCM formats). Commanded data rates are programmed by a series of bit rate grouped commands based on powers of 10.

As an example, the command sequence for commanding the LS-040 to a bit rate of 10,575,000 is shown below:

<u>Bit Rate Position</u>		<u>Formula</u>	<u>Command Set</u>
10,000,000	=	1x 10Mbps	0x91
1,000,000	=	0x 1Mbps	0x10
100,000	=	5x 100kbps	0x25
10,000	=	7x 10kbps	0x37
1,000	=	5x 1kbps	0x45
100	=	0x 100bps	0x50
10	=	0x 10bps	0x60
1	=	0x 1bps	0x70

0x0A (Master Configuration Command)

#### 4.2.3 Tentative Loop Bandwidth Commands (0x8\_)

The LS-040 allows the user to program the loop bandwidth (LBW) based on the expected input signal. A larger loop bandwidth setting allows the bit synchronizer a larger tracking and

acquisition range for less stable or more noise prone signals. Lower loop bandwidths are used for enhanced performance on more tightly controlled input signals.

Programming of the LBW setting is considered tentative. The user may elect to program any loop bandwidth that they desire. However, there are practical tracking and acquisition limits imposed by the LS-040 symbol tracker design. As an example, if a 2% LBW selection were programmed at a bit rate of 20Mbps, the loop would extend +/-400kHz around the desired input signal. The acquisition loop extends this loop to 4 times the LBW setting making the acquisition loop 1.6MHz. Due to practical limitations of the digital filters, this is beyond the programmable range for high data rates. Regardless of the commanded LBW setting, on-board software of the LS-040 will default the maximum bandwidth settings according to the values in Table 4-3. Table 4-4 provides a chart of commands for both the LS-040 and the corresponding setting for the SBS 4400-TF series analog bit synchronizer.

Bit Rate Range	Maximum LBW Setting
50bps ≤ Bit Rate < 400,010bps	2%
400,010bps ≤ Bit Rate < 800,010bps	1%
800,010bps ≤ Bit Rate < 1,600,100bps	0.5%
1,600,100bps ≤ Bit Rate < 3,200,100bps	0.2%
3,200,100bps ≤ Bit Rate < 5,000,100bps	0.1%
5,000,100bps ≤ Bit Rate < 10,001,00bps	0.05%
10,001,000bps ≤ Bit Rate < 20,000,00bps	0.02%

**Table 4-3 LS-040 Maximum LBW Settings based on programmed bit rate**

Loop Bandwidth (LBW) Commands (Hex)	LS-040 Setting	SBS 4400-TF Setting
0x80	(Invalid)	(Invalid)
0x81	0.1%	0.1%
0x82	0.2%	0.2%
0x83	0.2%	0.3%
0x84	0.2%	0.4%
0x85	0.5%	0.5%
0x86	0.5%	0.6%
0x87	0.5%	0.7%
0x88	1.0%	0.8%
0x89	1.0%	0.9%
0x8A	1.0%	1.0%
0x8B	2.0%	2.0%
0x8C	2.0%	3.0%
0x8D	0.01%	(Invalid)
0x8E	0.02%	(Invalid)
0x8F	0.05%	(Invalid)

**Table 4-4 LS-040 commands for LBW Settings**

#### 4.2.4 PCM Input Code Commands (0xA\_)

The LS-040 allows the user to program the PCM input decoder for a variety of input formats. The PCM decoder is used to translate the incoming PCM format to the provided NRZ-L output data format. Table 4-5 lists the common PCM decoder setup commands. Refer to Table 4-8 for additional PCM decoder command options.

PCM Input Decoder Commands (Hex)	Function
0xA0	PCM Input Decoder Selection: NRZ-L
0xA1	PCM Input Decoder Selection: NRZ-M
0xA2	PCM Input Decoder Selection: NRZ-S
0xA3	PCM Input Decoder Selection: BiΦ-L
0xA4	PCM Input Decoder Selection: BiΦ-M
0xA5	PCM Input Decoder Selection: BiΦ-S
0xA6	PCM Input Decoder Selection: DM-M
0xA7	PCM Input Decoder Selection: DM-S
0xA8	PCM Input Decoder Selection: Modified DM-M
0xA9	PCM Input Decoder Selection: Modified DM-S
0xAA	PCM Input Decoder Selection: Inv. NRZ-L
0xAB	PCM Input Decoder Selection: Inv. BiΦ-L
0xAC	PCM Input Decoder Selection: RZ
0xAD	PCM Input Decoder Selection: Inv. RZ
0xAE	PCM Input Decoder Selection: RNRZ-11
0xAF	PCM Input Decoder Selection: RNRZ-15

Table 4-5 LS-040 commands for PCM decoder and encoder settings

#### 4.2.5 PCM Output Code Commands (0xB\_)

The LS-040 allows the user to program the PCM output encoder for a variety of PCM output formats. The PCM encoder is used to translate the incoming PCM format to another desired PCM output data format. This is helpful for tape storage or may be used to accomplish PCM-to-PCM translation tasks. Table 4-6 lists the common PCM encoder setup commands. Refer to Table 4-8 for additional PCM encoder setup commands.

PCM Input Decoder Commands (Hex)	Function
0xB0	PCM Output Encoder Selection: NRZ-L
0xB1	PCM Output Encoder Selection: NRZ-M
0xB2	PCM Output Encoder Selection: NRZ-S
0xB3	PCM Output Encoder Selection: BiΦ-L
0xB4	PCM Output Encoder Selection: BiΦ-M
0xB5	PCM Output Encoder Selection: BiΦ-S
0xB6	PCM Output Encoder Selection: DM-M
0xB7	PCM Output Encoder Selection: DM-S
0xB8	PCM Output Encoder Selection: Modified DM-M
0xB9	PCM Output Encoder Selection: Modified DM-S
0xBA	PCM Output Encoder Selection: Inv. NRZ-L
0xBB	PCM Output Encoder Selection: Inv. BiΦ-L
0xBC	PCM Output Encoder Selection: RZ
0xBD	PCM Output Encoder Selection: Inv. RZ
0xBE	PCM Output Encoder Selection: RNRZ-11
0xBF	PCM Output Encoder Selection: RNRZ-15

Table 4-6 LS-040 commands for PCM decoder and encoder settings

## 4.2.6 Auxiliary Commands (0xC\_)

The LS-040 provides a set of auxiliary commands that allows additional features of the LS-040 to be enabled or disabled. Table 4-7 Lists these functions and associated reference paragraphs that define the commands in greater detail.

Auxiliary Commands (Hex)	Function	Reference Section
0xC0	Disable Auto-test at startup	4.2.6.1
0xC1	Enable Auto-test at startup	4.2.6.1
0xC2	2 <sup>11</sup> -1 PRN generator sequence	4.2.6.2
0xC3	2 <sup>15</sup> -1 PRN generator sequence	4.2.6.2
0xC4	NRZ-L Data and Clock Outputs Disabled at Symbol UNLOCK	4.2.6.3
0xC5	NRZ-L Data and Clock Outputs Disabled at Es/No < 5dB	4.2.6.3
0xC6	PCM Encoder Output Disabled at Symbol UNLOCK	4.2.6.3
0xC7	PCM Encoder Output Disabled at Es/No < 5dB	4.2.6.3
0xC8	Enable all PCM Output Sources	4.2.6.3
0xC9	External Link Analysis Testing Disabled	4.2.6.4
0xCA	External Link Analysis Testing Enabled	4.2.6.4
0xCB	Link Analysis Testing – Disable Forced Error	4.2.6.5
0xCC	Link Analysis Testing – Forced Error	4.2.6.5
0xCD	(Undefined)	
0xCE	(Undefined)	
0xCF	(Undefined)	

Table 4-7 LS-040 Auxiliary Function Commands

### 4.2.6.1 Disable/Enable Auto-test Commands (0xC0, 0xC1)

At the initiation of power to the LS-040, the unit initiates several Built-In-Test (BIT) functions. One of these tests wraps the on-board PRN generator to the PCM input of the device via the Auto-test relay. This in turn tests the functionality of over 95% of the unit's components. However, this period of testing disables the PCM input channel for several seconds. In some circumstances, a user may wish to disable this feature. The "Disable Auto-test at Startup" command (0xC0) disables this feature. The "Enable Auto-test at Startup" command (0xC1) enables this feature.

The LS-040 is shipped from the factory with this feature enabled. For most users, it is recommended that this feature remain enabled during normal use. The Auto-test feature completes long before most operating systems can establish normal control.

### 4.2.6.2 PRN Generator Pattern Commands (0xC2, 0xC3)

The LS-040 has a built-in Pseudo-Random Number (PRN) generator that is used as a data source for a PCM output channel used for self-test and link-analysis functions. The user is allowed to select the PRN "seed" function which determines the length of the PRN pattern that the generator will sequence through before repeating. The LS-040 provides two different pattern lengths: 2<sup>11</sup>-1 (2,047 bits) and 2<sup>15</sup>-1 (32,767 bits).

The user is allowed to select either pattern format by sending the "2<sup>11</sup>-1 PRN generator sequence" command (0xC2) or the "2<sup>15</sup>-1 PRN generator sequence" command (0xC3). The LS-040 defaults to the 2<sup>11</sup>-1 PRN pattern sequence if not otherwise commanded.

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#### **4.2.6.3 PCM, NRZ-L Clock and Data Output Commands (0xC4 - 0xC8)**

In certain operational environments, it may be desirable to disable the NRZ-L data and clock outputs, or the PCM encoder output, if the LS-040 symbol tracker is no longer locked or if the quality of the signal is very poor. In order to allow for this feature, the LS-040 provides four commands which will disable the clock and data outputs: “NRZ-L Data and Clock Outputs Disabled at Symbol UNLOCK” command (0xC4), the “NRZ-L Data and Clock Outputs Disabled at Es/No <5dB” command (0xC5), the “PCM Encoder Output Disabled at Symbol UNLOCK” command (0xC6), and the “PCM Encoder Output Disabled at Es/No <5dB” command (0xC7). The user can disable the data sources if the estimated PCM input signal-to-noise ratio Es/No is below 5dB or if the symbol tracker of the bit sync has entered an unlocked state. The user may opt to also maintain outputs regardless of the PCM input channel quality and only shut down the data/clock outputs if the LS-040 symbol tracker is unlocked.

The “Enable all PCM Output Sources” command (0xC8) re-initializes all clock and data output sources. The LS-040 is shipped from the factory with all sources enabled.

#### **4.2.6.4 External Link Analysis Testing Disable/Enable (0xC9, 0xCA)**

As an option, the LS-040 has the ability to perform an external link analysis function using its on-board PRN PCM pattern generator as illustrated in Figure 2-1. In order to enable the PRN generator, the user must command the LS-040 with the “External Link Analysis Testing Enabled” command (0xCA). To disable the external link analysis function, the user must command the LS-040 with the “External Link Analysis Testing Disabled”, command (0xC9).

The LS-040 is shipped with the external link analysis testing function disabled. If the Link Analysis option is not present, this command will be disregarded.

#### **4.2.6.5 Link Analysis Testing – Forced Error Commands (0xCB, 0xCC)**

In order to more accurately assess an external PCM link, it is often desirable to determine if forced errors are being relayed through the system. The LS-040 provides a means of forcing single-bit errors in the pseudo-random PCM pattern being generated. A single bit error is injected in the output test stream when the “Link Analysis Testing - Forced Error” command (0xCC) is issued. This forced error condition can be reset by issuing a “Link Analysis Testing- Disable Forced Error” command (0xCB).

The LS-040 is shipped with the forced error function disabled. If the Link Analysis option is not present, this command will be disregarded.

#### **4.2.7 Auxiliary PCM Code Commands (0xD\_)**

The LS-040 allows the user to program additional PCM input randomizer decoder formats and the two additional PCM output randomizer encoder formats. It also allows for the selection of several inverted PCM decoder formats. Since all 16 combinations are used for the common PCM programming commands, this additional command set is provided to allow less common PCM format needs. Table 4-8 lists the additional command sequences.

PCM Aux. Randomizer Commands (Hex)	Function
0xD0	PCM Input Decoder Selection: RNRZ-17
0xD1	PCM Input Decoder Selection: RNRZ-23
0xD2	PCM Input Decoder Selection: Inv. NRZ-M
0xD3	PCM Input Decoder Selection: Inv. NRZ-S
0xD4	PCM Input Decoder Selection: Inv. BiΦ-M
0xD5	PCM Input Decoder Selection: Inv. BiΦ-S
0xD6	PCM Input Decoder Selection: Inv. DM-M
0xD7	PCM Input Decoder Selection: Inv. DM-S
0xD8	PCM Input Decoder Selection: Inv. Modified DM-M
0xD9	PCM Input Decoder Selection: Inv. Modified DM-S
0xDA	PCM Input Decoder Selection: Inv. RNRZ-11
0xDB	PCM Input Decoder Selection: Inv. RNRZ-15
0xDC	PCM Input Decoder Selection: Inv. RNRZ-17
0xDD	PCM Input Decoder Selection: Inv. RNRZ-23
0xDE	PCM Output Encoder Selection: RNRZ-17
0xDF	PCM Output Encoder Selection: RNRZ-23

**Table 4-8 LS-040 Auxiliary Commands for PCM Code Settings**

#### 4.2.8 Status Commands (0xE\_)

The LS-040 allows reverse transfer of data from the LS-040 to the host processor via the parallel or serial bus interface. All status commands result in a response which first echoes the original status command followed by the status characters associated with the command (refer to Figure 4-2). Table 4-9 lists the functions of these commands and provides a reference section for further command response definitions.

Status Commands (Hex)	Function	No. of Status Characters	Reference Section
0xE0	Product Configuration/Identification Status	3	4.2.8.1
0xE1	Programmed PCM Bit Rate Status	8	4.2.8.2
0xE2	Bit Sync Operational Status	4	4.2.8.3
0xE3	Link Analysis Update Status	1	4.2.8.4
0xE4	Link Analysis Operational Status	3	4.2.8.5
0xE5	Link Analysis Bit Count Status	3	4.2.8.6
0xE6	Link Analysis Error Count Status	2	4.2.8.7
0xE7	PCM Input Decoder Status	1	4.2.8.8
0xE8	PCM Output Encoder Status	1	4.2.8.9
0xE9	BIT Status	5	4.2.8.10
0xEA	Offset Frequency Status	7	4.2.8.11
0xEB	Signal Voltage Status	7	4.2.8.12
0xEC	Estimated Es/No Status	7	4.2.8.13
0xED	LBW Setting Status	1	4.2.8.14
0xEE	(Undefined)		
0xEF	(Undefined)		

**Table 4-9 LS-040 Status Commands**

### 4.2.8.1 Product Configuration/Identification Status Command (0xE0)

The “Product Configuration/Identification Status” command (0xE0) provides a 4-character status containing information on the configuration of the LS-040. Status contents include the maximum NRZ data rate limit of the device as well as any other configuration options. Figure 4-10 defines the status returned by this command.

Status Byte	Status Value (Hex)	Status Definition
1	0x20	20Mbps (NRZ) LS-040 Version
	0x10	10Mbps (NRZ) LS-040 version
2	0x01	Link Analysis Option Present
	0x00	Link Analysis Option Not Present
3	0x00	(Future Growth)
4	0x00	(Future Growth)

Table 4-10 LS-040 Product Identification/Configuration Status Response

### 4.2.8.2 Programmed PCM Bit Rate Status Command (0xE1)

The “Programmed PCM Bit Rate Status” command (0xE1) provides an 8-character status response containing information on the present PCM input rate setting for the LS-040. Table 4-11 defines the status returned by this command.

Status Byte	Status Value (Hex)	Status Definition
1	0x9_	Lower nibble = PCM Bit Rate Command (x10 Mbps) [0..2 range]
2	0x1_	Lower nibble = PCM Bit Rate Command (x1 Mbps) [0..9 range]
3	0x2_	Lower nibble = PCM Bit Rate Command (x100kbps) [0..9 range]
4	0x3_	Lower nibble = PCM Bit Rate Command (x10kbps) [0..9 range]
5	0x4_	Lower nibble = PCM Bit Rate Command (x1kbps) [0..9 range]
6	0x5_	Lower nibble = PCM Bit Rate Command (x100bps) [0..9 range]
7	0x6_	Lower nibble = PCM Bit Rate Command (x10bps) [0..9 range]
8	0x7_	Lower nibble = PCM Bit Rate Command (x1bps) [0..9 range]

Table 4-11 PCM Bit Rate Status Response

### 4.2.8.3 Bit Sync Operational Status (0xE2)

The “Bit Sync Operational Status” command (0xE2) provides a 4-character status response containing information on the PCM input signal and the results of the continuous BIT functions performed by the on-board DSP. Table 4-12 defines the status returned by this command.

Status Byte	Status Value (Hex)	Status Definition
1	0x10	PCM Input Signal below the input threshold detection level
	0x11	PCM Input Signal within the threshold range
2	0x20	Bit Sync PLL Unlocked
	0x21	Bit Sync PLL Locked
3	0x30	PCM Input Signal Quality – Below threshold (Es/No < 5dB)
	0x31	PCM Input Signal Quality – Above threshold (Es/No >=5dB)
4	0x40	BIT Errors – No errors reported
	0x41	BIT Errors – Errors being detected

**Table 4-12 Bit Sync Operational Status Response**

**4.2.8.4 Link Analysis Update Status (0xE3)**

The “Link Analysis Update Status” command (0xE3) provides a 1-character status response containing information on the PRN bit count and error count update status. If this status indicates that counter values have been updated, the user should issue the “Link Analysis Bit Count Status” command (0xE5) and the “Link Analysis Error Count Status” command (0xE6). Dividing the error count by the bit count will provide the BER rate recorded. Table 4-13 Defines the status returned by this command.

Status Byte	Status Value (Hex)	Status Definition
1	0x00	The Bit Count and Error Count Values have not been updated
	0xFF	The Bit Count and Error Count Values are updated

**Table 4-13 Link Analysis Update Status Response**

**4.2.8.5 Link Analysis Operational Status (0xE4)**

The “Link Analysis Operational Status” command (0xE4) provides a 3-character status response containing information on the Link Analysis pattern tracking and correlation within the LS-040. This information is critical in determining the validity of the link analysis calculations. Table 4-14 defines the status returned by this command.

Status Byte	Status Value (Hex)	Status Definition
1	0x10	The PRN Pattern is Locked
	0x11	The PRN Pattern is Unlocked
2	0x20	PRN Pattern Synchronization Maintained Since Update
	0x21	PRN Pattern Synchronization Lost Since Last Update
3	0x30	No Error Count Overflow
	0x31	Error Count Overflow

**Table 4-14 Link Analysis Operational Status Response**

#### 4.2.8.6 *Link Analysis Bit Count Status (0xE5)*

The “*Link Analysis Bit Count Status*” command (0xE5) provides a 4-character status response containing the actual bit count of the PRN correlator. Each of the 4-characters contains a portion of the hexadecimal representation of the overall bit count. The LS-040 contains a 26-bit bit counter. The first character contains the 8-LSBs of the bit count. The fourth character contains the 2-MSBs of the bit count.

#### 4.2.8.7 *Link Analysis Error Count Status (0xE6)*

The “*Link Analysis Error Count Status*” command (0xE6) provides a 3-character status response containing the actual error count observed by the internal PRN correlator. Each of the 3-characters contains a portion of the hexadecimal representation of the overall error count. The LS-040 contains a 20-bit error counter. The first character contains the 8-LSBs of the error count. The third character contains the 4-MSBs of the bit count.

#### 4.2.8.8 *PCM Input Decoder Status (0xE7)*

The “*PCM Input Decoder Status*” command (0xE7) provides a 1-character status response containing the programmed PCM decoder settings. The status value returned will be the same as that used for programming the desired PCM Input Decoder settings listed in Table 4-5 and Table 4-8.

#### 4.2.8.9 *PCM Output Encoder Status (0xE8)*

The “*PCM Output Encoder Status*” command (0xE8) provides a 1-character status response containing the programmed PCM Encoder settings. The status value returned will be the same as that used for programming the desired PCM Output Encoder settings listed in Table 4-6 and Table 4-8.

#### 4.2.8.10 *BIT Status (0xE9)*

The “*BIT Status*” command (0xE9) provides a 5-character status response containing information on the Built-In-Test functions that are being performed by the on-board DSP. Table 4-15 defines the different status bytes returned. This table also refers to additional sub-tables which contain further bit definitions for each status byte.

Status Byte	Reference Table	Status Definition
1	4-15A	Overall BIT Status
2	4-15B	Serial Interface Status

3	4-15C	Internal SW Version Status
4	4-15D	Synchronization and PCM Generation Status
5	4-15E	Power Monitoring Status

**Table 4-15 BIT Status Byte Response Reference**

Bit	Definition	Details	Logic State
0	Overall Health Flag	Logical "AND" of bits 1 to 5	1 = PASS, 0 = ERROR
1	Power-Up BIT Error	Results of Power-Up BIT	1 = PASS, 0 = ERROR
2	(Unused)	(Reserved)	1
3	Hardware Error	Synchronization and PCM Generation Status	1 = PASS, 0 = ERROR
4	Serial Error	Periodic monitoring of serial TX/RX channel	1 = PASS, 0 = ERROR
5	Power Source Error	Periodic monitoring of power supplies	1 = PASS, 0 = ERROR
6	(Unused)	(Reserved)	1
7	Synchronization Flag	Periodic Check of the Synchronization State	1 = PASS, 0 = ERROR

**Table 4-15A Overall BIT Status Byte Definition**

Bit	Definition	Details	Logic State
0	(Unused)	(Reserved)	1
1	Parity Error	Serial Receiver detected a Parity Error	1 = PASS, 0 = ERROR
2	Syntax Error	Serial Receiver detected a Syntax Error	1 = PASS, 0 = ERROR
3	Semantic Error	Semantic error in command detected	1 = PASS, 0 = ERROR
4	Overflow	Serial receiver detected an overflow condition	1 = PASS, 0 = ERROR
5	(Unused)	(Reserved)	1
6	(Unused)	(Reserved)	1
7	(Unused)	(Reserved)	1

**Table 4-15B Serial Interface Status Byte Definition**

Bit	Definition	Comments
0	Internal SW Version Identification (lsb)	(Consult Factory for details)
1	Internal SW Version Identification	
2	Internal SW Version Identification	
3	Internal SW Version Identification	
4	Internal SW Version Identification	
5	Internal SW Version Identification	
6	Internal SW Version Identification	
7	Internal SW Version Identification (msb)	

**Table 4-15C Internal Software Version Status Byte Definition**

Bit	Definition	Details	Logic State
0	Test Results	(Reserved)	1 = PASS, 0 = ERROR
1	Symbol Tracker	State of Symbol Tracking Loop	1 = SYNC, 0 = NO SYNC
2	Offset Frequency	State of offset frequency <5%	1 = PASS, 0 = ERROR
3	Es/No Within Range	Estimated Es/No >= 5dB	1 = PASS, 0 = ERROR

4	Signal Within Range	Input Signal within Range	1 = PASS, 0 = ERROR
5	(Unused)	(Reserved)	1
6	Link Analysis Active	Indicates that Link Analysis functions are Active	1 = ACTIVE, 0 = INACTIVE
7	(Unused)	(Reserved)	1

Table 4-15D Synchronization and PCM Generation Status Byte Definition

Bit	Definition	Details	Logic State
0	VCC (5VDC)	Voltage within +/- 10% of nominal value	1 = PASS, 0 = ERROR
1	+12VDC	Voltage within +/- 10% of nominal value	1 = PASS, 0 = ERROR
2	-12VDC	Voltage within +/- 10% of nominal value	1 = PASS, 0 = ERROR
3	+5VDC (Analog Ref.)	Voltage within +/- 10% of nominal value	1 = PASS, 0 = ERROR
4	-5VDC (Analog Ref.)	Voltage within +/- 10% of nominal value	1 = PASS, 0 = ERROR
5	+3.3VDC	Voltage within +/- 10% of nominal value	1 = PASS, 0 = ERROR
6	(Unused)	(Reserved)	1
7	(Unused)	(Reserved)	1

Table 4-15E Power Monitoring Status Byte Definition

#### 4.2.8.11 Offset Frequency Status (0xEA)

The “Offset Frequency Status” command (0xEA) provides a 7-character status response containing the offset frequency that the LS-040 is detecting from the programmed bit rate. This information is useful in determining signal integrity and in evaluating loop stress. The frequency offset is reported over a range of +/-20% in a scientific format. As an example, status bytes associated with a +1% frequency error status response is shown in Table 4-16.

Status Byte	Byte Value (Hex)	Status Definition
1	0x2B	ASCII Character “+”
2	0x31	ASCII Character “1”
3	0x2E	ASCII Character “.”
4	0x30	ASCII Character “0”
5	0x45	ASCII Character “E”
6	0x2D	ASCII Character “-”
7	0x32	ASCII Character “2”

Table 4-16 Example Offset Frequency Status Response

#### 4.2.8.12 Signal Voltage Status (0xEB)

The “Signal Voltage Status” command (0xEB) provides a 7-character status response containing the *estimated* PCM input signal level. This information is useful in determining signal integrity. The signal voltage is report over a range of 0.1V to 10V p-p % in a scientific format. As an example, status bytes associated with a 3.0V signal voltage status response is shown in Table 4-17.

Status Byte	Byte Value (Hex)	Status Definition
1	0x2B	ASCII Character "+"
2	0x33	ASCII Character "3"
3	0x2E	ASCII Character "."
4	0x30	ASCII Character "0"
5	0x45	ASCII Character "E"
6	0x2B	ASCII Character "+"
7	0x30	ASCII Character "0"

**Table 4-17 Example Signal Voltage Status Response**

#### 4.2.8.13 Signal Voltage Status (0xEC)

The "Estimated Es/No Status" command (0xEC) provides a 7-character status response containing the **estimated** signal-to-noise ratio Es/No of the PCM input signal. This information is useful in determining signal integrity. The Es/No is report over a range of -5dB to +20dB in a scientific format. As an example, status bytes associated with a +13dB estimated Es/No status response is shown in Table 4-18.

Status Byte	Byte Value (Hex)	Status Definition
1	0x2B	ASCII Character "+"
2	0x31	ASCII Character "1"
3	0x2E	ASCII Character "."
4	0x33	ASCII Character "3"
5	0x45	ASCII Character "E"
6	0x2B	ASCII Character "+"
7	0x31	ASCII Character "1"

**Table 4-18 Example Estimated Es/No Level Status Response**

#### 4.2.8.14 LBW Setting Status (0xED)

The "LBW Setting Status" command (0xED) provides a 1-character status response containing the **actual** LS-040 PLL loop bandwidth (LBW) setting. Since all LBW settings commanded by the user are range checked in accordance with the PCM input bit rate setting, the reported setting will be the larger of either the user commanded value or the value from Table 4-3. The values reported will be the same as those found in Table 4-4.

### 4.2.9 Address Commands (0xF\_)

The LS-040 has provisions for addressing more than one module via a single host command interface. To utilize this function, three elements **MUST** be in place:

1. The user must address each module with a unique address from 1 to 15 via switch S1-3 through S1-6 (reference Figure 3-6). Switch S1 selects the lower address nibble in accordance with Table 4-19. Module address 0x0 is reserved for cases where multi-addressing is not used.
2. The user must insert address commands prior to the “*Master Configuration Command*” (0x0A) as shown in Figure 4-2.
3. The use of a single IEEE1284 or EIA232 style interface to command multiple units **REQUIRES** the use of special control hardware to handle the electrical interfaces and the handshake arrangements. The description of this specialized control hardware is beyond the scope of this manual. Consult the factory for additional details.



**Warning:** The use of the multi-addressing command sequences requires the use of unique addresses for each module. Failure to provide unique addresses will result in undesirable effects.



**Warning:** The use of the multi-addressing configurations without the use of specialized control hardware may result in hardware failures.

Addressing Commands	Function
<b>0xF0</b>	Multi-address command function disabled
<b>0xF1</b>	Commands addressed to Module Address 1
<b>0xF2</b>	Commands addressed to Module Address 2
<b>0xF3</b>	Commands addressed to Module Address 3
<b>0xF4</b>	Commands addressed to Module Address 4
<b>0xF5</b>	Commands addressed to Module Address 5
<b>0xF6</b>	Commands addressed to Module Address 6
<b>0xF7</b>	Commands addressed to Module Address 7
<b>0xF8</b>	Commands addressed to Module Address 8
<b>0xF9</b>	Commands addressed to Module Address 9
<b>0xFA</b>	Commands addressed to Module Address 10
<b>0xFB</b>	Commands addressed to Module Address 11
<b>0xFC</b>	Commands addressed to Module Address 12
<b>0xFD</b>	Commands addressed to Module Address 13
<b>0xFE</b>	Commands addressed to Module Address 14
<b>0xFF</b>	Commands addressed to Module Address 15

**Table 4-19 LS-040 Addressing Commands**