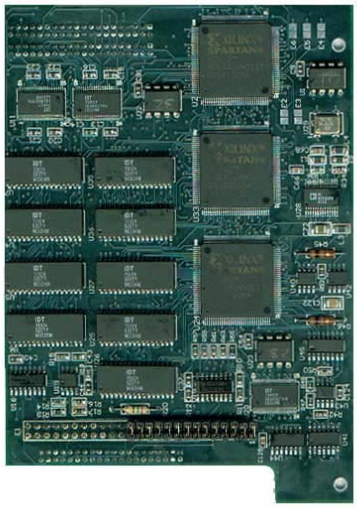
LUMISTAR

LS-55-DB Multi-function PCM Decommutator Daughterboard

Data Sheet

Description:

The Lumistar LS-55-DB Multi-function PCM Decommutator Daughterboard is designed to be used on the LS-50-P PCI Multi-function Decommutator, LS-50-V VME Multi-function Decommutator, or the LS-50-cP Compact PCI Multi-Function Decommutator allowing an increased number of functions in a single card slot. When used along with the LS-40-DB Bit Synchronizer Daughterboard on the LS-50-P PCI Multi-Function Decom, 11 functions typically encountered in test applications can be achieved in a single PCI card slot. The two daughterboards are used to enhance the capability of the five functions of the main PCI board (PCM Simulator, PCM Decommutator, IRIG Time Code Generator, IRIG Time Code Reader, and Bit Error Tester). When used on the LS-50-V VME Multi-function Decom or the LS-50-cP Compact PCI Multi-function Decom, up to 10 functions are achieved in a single Compact PCI slot.



The Slave IRIG Time Code Reader on the LS-55-DB accepts the digitized IRIG time code signal from the Time Code Reader on the LS-50-P, LS-50-V, or LS-50–cP board and allows time tagging the PCM data blocks of the data being decommutated by the daughterboard. The Time Code Generator creates and outputs time information in accordance with IRIG Time Code Standards. The Lumistar LS-55-DB Decom can be used for extremely large formats (65,530 words per minor frame up to 1,024 frames deep) and contains dual ping-pong data output buffers with up to 128K bytes of memory. The LS-55-DB decom can be used for an independent PCM data stream or an embedded PCM data stream in accordance with the IRIG-106 Standards. The PCM simulator can generate complex data streams with embedded PCM data or two totally independent data streams.

Key Features:

- **Adds 5 functions to LS-50-P, LS-50-V, or LS-50-cP Multi-function Decoms**
    1. **PCM Simulator**
    2. **PCM Decommutator**
    3. **Slave IRIG Time Code Reader**
    4. **IRIG Time Code Generator**
    5. **BERT with error injection capability (Optional)**

Please note that the LS-55-DD Dual Multi-function Decom achieves the same results as the earlier LS-50-P with the LS-55-DB in a short PCI board.

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SPECIFICATIONS:

PCM DECOMMUTATOR:

Input Data Rate	64.0 bps to 20.0 Mbps
Input Signals	NRZ-L data & 0 degree clock
Input Levels	Single-ended TTL & RS-422
Word Length (VWL)	Variable from 3 to 16 bits per word on a word-by-word basis
CRC checker	CRC16/CCITT Forward/Reverse
Minor Frame Length	2 to 65,530 words per frame
Major Frame Length	Up to 1024 minor frames per major frame
Bit Order	MSB or LSB-first (word-by-word basis)
Frame Sync Pattern	Up to 64 bits (any pattern with don't care bits (X) may be used)
Frame Sync Location	Beginning or end of the frame
Frame Sync Strategy	Adaptive mode (search-lock-verify) & burst mode (search-lock)
Sync Error Tolerance	0 to 15 bits (selectable)
Sync Slip Window	1 or 3 bits wide (selectable)
Data Polarity	Normal, inverted or automatic
Subframe Sync	FCC (FAC), SFID or URC (Optional)
URC Location	Any 32 bit window within the first minor frame not including the last bit in the minor frame
SFID Location	Any series of contiguous bits not including the last bit in the minor frame
System Output	Buffered output with status, time, & data

IRIG A/B/G READER/GENERATOR:

Time Reader Input Format	IRIG A, B, or G
Input signal level	1V p-p nominal
Latency	2µsec (maximum)
Data Outputs	Automatic time tags for PCM data blocks (time accessible in register space)
Time Generator Output	IRIG A, B, or G
Pulse Output	1 pps
Flywheel	1/2x, 1x, 2x

MECHANICAL:

Daughterboard Form Factor	Custom Daughterboard Compatible with LS-50-P, LS-50-V, and LS-50-cP

PCM SIMULATOR:

Outputs	Data, 0 & 90 degree clocks & minor frame strobes
Output Levels	Single-ended TTL & RS-422
Output Data Rate	64.0 bps to 20.0 Mbps (NRZ codes) 64.0 bps to 10.0 Mbps (all other codes)
PCM Codes	NRZ-L/M/S BIϕ-L/M/S DM-M/S RNRZ-L (2^{11}-1, 2^{15}-1)
Word Length (VWL)	Variable from 3 to 16 bits per word on a word-by-word basis
CRC Generator	CRC16/CCITT
Minor Frame Length	2 to 65,530 words per frame
Major Frame Length	Up to 1024 minor frames per major frame
Bit Order	MSB or LSB-first on a word-by-word basis
Frame Sync Pattern	Up to 64 bits (any series of 0s or is 1s may be used)
Sub-Frame Sync	FCC (FAC), SFID & URC; URC location may be any 64 bit window within the first minor frame not including the last bit in the minor frame
Common Words	May be a single value or selected from a group of one minor frame or 16,384 words whichever is less. Data may be changed while operating.
Unique Words	Seven may be programmed in any mainframe, super-commutated, or subcommutated channel. Data may be changed while operating.
Waveform Words	Five may be programmed to appear in every frame at the same location. Data may be changed while operating.

ENVIRONMENTAL:

Temperature (Operating)	0 to 50 °C
Temperature (Non-Op)	-25 to +70 °C
Humidity (Operating)	10% to 90% Non-Condensing
Humidity (Non-Op)	Packaging must prevent contact with moisture and contaminants
Special Handling	Standard ESD methods required

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