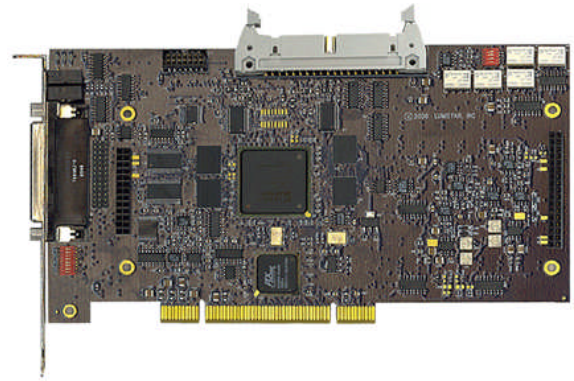


LUMISTAR

LS-55-DD PCI Dual Multi-function PCM Decommutator Data Sheet

Description:

The Lumistar LS-55-DD PCI Dual Multi-function PCM Decommutator offers two multifunction decoms and one optional bit synchronizer in a single PCI card slot. The multi-function decoms are implemented in FPGA using a next generation design based on the LS-50-P. The simulators, decommutators, time code reader and time code generator are achieved on the main board and the bit synchronizer is achieved through a low-profile daughterboard. CVSD voice, h.261 video, and IRIG Chapter 8 decoding are achieved through software.



The IRIG Time Code Reader and Generator operate with IRIG A, B, or G time codes. The Time Code Reader is typically used to insert time information into the PCM minor frame block of data. The Time Code Generator creates and outputs time information in accordance with the IRIG Time Code Standards. Both reader and generator are capable of operating at ½, 1, and 2 times the normal rate.

The dual decoms can be used for extremely large formats (65,536 words per minor frame up to 1,024 frames deep) and contains dual ping-pong data output buffers with up to 128K bytes of memory. The second decom can be used for an independent PCM data stream or an embedded data stream in accordance with the IRIG-106 Standard.

The dual PCM simulator generates common, unique, and waveform pattern data words or pseudo-random test pattern (11 through 25 bit) to allow bit error loop calculations to be performed. The two simulators can be used to generate complex data streams with embedded PCM data, or two totally independent data streams. Five-pole Butterworth pre-modulation filtering is provided with 8 selectable data rates on each simulator from 100 Kbps to 20 Mbps.

Key Features: Dual PCI Multifunction PCM Decommutator contains

- 2 PCM Simulators with pre-mod filtering and BERT generating capability
- 2 PCM Decommutators with BERT reading capability
- IRIG Time Code Reader and IRIG Time Code Generator
- LS-40-DB Bit Synchronizer Daughterboard - Optional (10, 20, 25 Mbps)
- Additional Bit Synchronizer using LS-40-B Drive Bay giving two streams in one slot
- CVSD Voice, h.261 Video, and IRIG Chapter 8 Decoding through LDPS-Pro Software
- Short PCI Board only 7.55 inches long

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SPECIFICATIONS:

PCM DECOMMUTATORS (2):

Input Data Rate	64 bps to 30 Mbps
Input Signals	NRZ-L data & 0 degree clock
Input Levels	Single-ended TTL & RS-422
Word Length (VWL)	Variable from 3 to 16 bits per word on a word-by-word basis
CRC checker	CRC16/CCITT
Minor Frame Length	2 to 65,536 words per minor frame
Major Frame Length	Up to 1024 minor frames per major frame
Bit Order	MSB or LSB-first (word-by-word basis)
Frame Sync Pattern	Up to 64 bits (any pattern with don't care bits (X) may be used)
Frame Sync Location	Beginning or end of the frame
Frame Sync Strategy	Adaptive mode (search-lock-verify) & burst mode (search-lock)
Sync Error Tolerance	0 to 15 bits (selectable)
Sync Slip Window	1, 3, 5, or 7 bits wide (selectable)
Data Polarity	Normal, inverted or automatic
Subframe Sync	FCC (FAC), SFID or URC (Optional)
URC Location	Any 64 bit window within the first minor frame not including the last bit in the minor frame
SFID Location	Any series of contiguous bits not including the last bit in the minor frame

IRIG A/B/G READER/GENERATOR (1):

Time Reader Input Format	IRIG A, B, or G
Time Reader Rate	½, 1, or 2 times normal rate
Input signal level	1V p-p nominal
Latency	2µsec (maximum)
Data Outputs	Automatic time tags for PCM data blocks (time accessible in register space)
Time Generator Output	IRIG A, B, or G
Time Generator Rate	½, 1, or 2 times normal rate

MECHANICAL:

PCI	PCI Board 7.55" Long
Daughterboard Form Factor	LS-40-DB for Bit Synchronizer

POWER REQUIREMENTS:

5V	850 ma
-12 V	120 ma
+12V	30 ma

PCM SIMULATORS (2):

Outputs	Data, 0 degree clock & minor frame strobes
Output Levels TTL, 422	Single-ended TTL or RS-422 levels on PCM Data and Clock
Base-band Output	200 mV to 8 V p-p adjustable
Base-band Pre-mod Filter	8 on each simulator
Output Data Rate	Selectable; 5-pole Butterworth
PCM Codes	64 bps to 30 Mbps (NRZ codes)
Word Length (VWL)	64 bps to 15 Mbps (all other codes)
CRC Generator	NRZ-L/M/S, BIφ-L/M/S
Minor Frame Length	DM-M/S, RNRZ-L (2 ¹¹ -1, 2 ¹⁵ -1)
Major Frame Length	Variable from 3 to 16 bits per word on a word-by-word basis
Bit Order	CRC16/CCITT
Frame Sync Pattern	2 to 16,383 words per minor frame
Sub-Frame Sync	Up to 1024 minor frames per major frame
Common Words	MSB or LSB-first on a word-by-word basis
Unique Words	Fully programmable
Waveform Words	Fully Programmable
	May be a single value or selected from a group of one minor frame or 2048 words whichever is less.
	Seven may be programmed in any mainframe, super-commutated, or subcommutated channel.
	Five may be programmed to appear in every frame at the same location.

BERT:

Pseudo-random patterns	11, 15, 17, 19, 21, 23, and 25
Bit Error Rate	Indicated on Software
Error Count	Indicated on Software
Forced Error Modes	Continuous Forced Error
History Log	Single Bit Forced Error
	Yes

ENVIRONMENTAL:

Temperature (Operating)	10 to 50 °C
Temperature (Non-Op)	-25 to +70 °C
Humidity (Operating)	10% to 90% Non-Condensing
Humidity (Non-Op)	Packaging must prevent contact with moisture and contaminants
Special Handling	Standard ESD methods required

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Specifications are subject to change. Please verify the latest specifications at time of order.

4-15-08